
# Silicon Valley Polytechnic Institute

## SCHOOL CATALOG

**FOR**

**CALENDAR YEAR**

## 2014-2015

**1762 Technology Drive, Suite 228**
**San Jose, CA 95110**

# Silicon Valley Polytechnic Institute

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## THE MISSION, PURPOSES

The mission and objectives of the Silicon Valley Polytechnic Institute (SVPTI) are as follows:

It is the mission of the SVPTI to achieve and maintain a position as a leading training provider serving the electronic and computer industries. SVPTI strives to provide students with a fostering, productive and professional training environment that maximizes the learning process. The instruction provided for students is high quality and highly individualized. It is intended to develop and enhance the knowledge and demanding skills required in these exceptionally dynamic fields.

SVPTI intends to achieve its mission by offering highly useful non-degree certificate and diploma programs using relevant, focused and advanced curricula, a high level of student – instructor interaction, small class sizes and highly qualified faculty with years of direct industry experience.

Silicon Valley Polytechnic Institute strives to provide students with a fostering, productive and professional training environment that maximizes the learning process. The instruction provided for students is high quality and highly individualized. It is intended to develop and enhance the knowledge and demanding skills required in these exceptionally dynamic fields.

Non-Degree programs at present include forty programs in total. Representative programs include: Computer Aided Design and Drafting with AutoCAD; Advanced and 3D Computer Drafting and Design with AutoCAD; Computer Aided Design and Drafting with SolidWorks: Advanced Computer Aided Design and Drafting with SolidWorks; Digital VLSI Design with Verilog; Timing Verification of Digital VLSI Designs; Design of Analog CMOS Integrated Circuits; and Design of Radio Frequency Integrated Circuits.

Students at SVPTI are very predominantly working professionals who often have diplomas and degrees. These students have typically been employed for a period of at least 2 to 3 years.

SVPTI primarily serves the demographic above because there is such dynamic change in the industrial sector that an employee needs to periodically update and re-tool their knowledge and skills.

SVPTI will maintain strong ties with the electronic, computer and Internet industries to constantly improve its training products and procedures and to be responsive to the needs of these changing industries. It is anticipated that an Industry Advisory Committee will be established perhaps within the first year of operations.

SVPTI is careful not to make specific occupation or job guarantees or promises of placement made upon graduation from a course or program. Obviously, there are a range of occupations or titles to which such training may lead. Though no specific guarantees of employment and no promises of placement are made, there are numerous related occupations or job titles that require such knowledge and skills provided through the courses and programs at SVPTI.

Students do not need to be licensed technicians or engineers to obtain a large number of available jobs in the general field of electrical engineering. Representative occupations for which graduates of SVPTI programs would be qualified include the following in the general field of electrical engineering:

- Analog Design Engineering
- Radio Frequency and Integrated Circuits Engineering (RFIC)
- Digital Design Engineering
- Computer Aided Design Drafting
- Computer Aided Design Drafting – Sheet Metal Engineering
- Computer Aided Design Drafting – Architectural Engineering

It is the policy of SVPTI that all newly enrolled students will receive a copy of the then current school catalog as part of their enrollment process. SVPTI recognizes that an enrollment agreement is not valid absent the student receiving a current school catalog prior to signing. The catalog will be available online for ready reference, or, if the student wishes to obtain a hard copy of the catalog, one will be provided upon request.

Additionally the policy of SVPTI is that the school catalog will be periodically updated as necessary with catalog addenda. However, all catalogs will otherwise be updated and republished as a new edition at least every two years. The period covered by any particular catalog will be clearly stated on the cover/title page of the catalog.
In addition to receiving the school catalog, which contain outline of all training programs, if necessary students might receive a program specific brochure from school and/or from the program's instructor if available.

As a prospective student, you are encouraged to review this catalog prior to signing an enrollment agreement. You are also encouraged to review the School Performance Fact Sheet which must be provided to you prior to signing an enrollment agreement.

## PROGRAMS OF INSTRUCTION

Silicon Valley Polytechnic Institute offers forty courses of instruction. All of the program offerings are centered on the subject area of electrical engineering and software. This instruction is highly technical.

All programs are 12 weeks (120 Hours) in length.
There are no requirements for licensure to work in any of the subject areas of instruction.

The partial list of current programs of instruction includes:

1 Computer Aided Design and Drafting with AutoCAD
2 Advanced and 3D Computer Drafting and Design with AutoCAD
3 Mechanical Drafting Fundamentals
4 3D Computer Aided Design and Drafting with SolidWorks
5 Advanced 3D Computer Aided Design and Drafting with SolidWorks
6 Autodesk Revit Architecture Essentials
7 Computer and Network Security Essentials
8 Software Quality Assurance Essentials

9 Solar Photovoltaic System Design Essentials
10 Advanced Solar Photovoltaic System Design
11 Advanced Semiconductor Devices - Physics & TCAD
12 Solar Photovoltaic Device Physics
13 Advanced Semiconductor Technology and Fabrication
14 Applied Electricity and Electronics Fundamentals
15 National Electrical Code (NEC) Training
16 Digital Logic Design Fundamentals
17 MATLAB for Engineering and Scientific Applications
18 IC Layout Design
19 IC Layout Verification
20 MEMS Design & Technology Fundamentals
21 PCB and PWB Technology Fundamentals
22 PCB Layout Design
23 Advanced PCB Layout Design
24 IC Packaging Fundamentals
25 IC Packaging Design Essentials
26 Digital Signal Processing Principles and Applications
27 Digital Signal Processing with MATLAB
28 Embedded System Design Fundamentals
29 Practical Design with DSP
30 FPGA Design Fundamentals
31 Automated Test and Measurement with LabVIEW
32 Digital VLSI IC Design with Verilog
33 Timing Verification of Digital VLSI Designs
34 Design of Digital CMOS Integrated Circuits
35 Design of Analog CMOS Integrated Circuits
36 Advanced Analog CMOS IC Design
37 Design of Radio Frequency Integrated Circuits
38 Advanced RFIC Design
39 Design of Low Power Digital Integrated Circuits
40 Low Power VLSI Design

Though various components of instruction can be supplemented by referencing the same subject matter on the Internet, all instruction at SVPTI is very much a combination of lecture and “hands on” instruction considered as “in residence” or face-to-face instruction.

These programs of instruction are described in much more detail on the following pages.

## SVPTI Programs

Appendix I of this catalog includes detail description of all the courses offered, as well as description of the instruction for each course offered by SVPTI. Training programs

consist of 1 of several of the courses taken together. Total clock hours for each course is120.

## SCHEDULE OF TOTAL CHARGES

| | |
|---|---|
| Tuition | $3000 per course |
| Registration Fee | N/A |
| STRF Fee | *NA |
| Leave of Absence Fee | N/A |
| Textbooks or Materials Charges | Student is responsible for purchasing necessary textbooks. Estimated charges: |

*After January 1 2015 schools shall discontinue collecting STRF assessments.
Tuition for all courses is $3000 per course.

## FACULTY AND QUALIFICATIONS

Among other things, California Code of Regulations Section 71720 states that an institution must employ duly qualified faculty in sufficient numbers to provide the instruction, student advisement, and learning outcomes evaluation necessary for the institution to document its achievement of its stated mission and objectives, and for students to achieve the specific learning objectives of each course offered.

It requires each institution to develop and implement written policies and procedures providing for the participation of duly qualified faculty in the conducting of research, development of curricula, academic planning, enforcement of standards of academic quality, pursuit of academic matters related to the institution's mission and objectives, establishment of criteria for contracting with new faculty, and evaluation of faculty credentials.

This section provides that the institution shall base its faculty requirements on all of the following factors:

1. The educational level and number of students;
2. The number of hours needed for direct interaction between students and faculty per course, quarter, semester, or other term;
3. The number of hours needed to be spent on evaluating written materials prepared by students, such as lessons, papers, and examinations, per course, quarter, semester, or other term;
4. The number of group meetings per course, quarter, semester, or other term;
5. The faculty duties established by the institution as required; and
6. The number of hours per week or units per term considered full-time for faculty in the institution. This section further provides that faculty shall possess sufficient expertise to support the institution's award of its degrees or diplomas, and that the faculty as a whole shall possess a diverse educational background. This diverse background shall be demonstrated by earned degrees from a variety of colleges and universities or by credentials generally recognized in the field of instruction.

Records document that each faculty member is duly qualified and was qualified to perform the duties to which they were assigned including providing instruction, and evaluating learning outcomes.

Appendix –II of this catalog includes a listing and qualification of additional faculty members.

Instruction will take place on the school premises. Instructors will of course be present at the school location when teaching, but instructors will also be available to meet with students outside of or in addition to class time during mutually agreed upon meeting times each week.

Due to the nature of the material covered, and the relatively small number of students per course, on average and across courses, this is expected to involve perhaps one additional hour per course per week.

## ADMISSION REQUIREMENTS

For approved Non-Degree programs, SVPTI will require applicants to have a high school diploma or its equivalent GED (General Education Diploma).

All applicants will be required to be at least 17 years of age by the commencement date of the first class in which they enroll. Documentation of age may be required.

Prospective students will meet with a SVPTI admissions representative on campus. All applicants must complete an Application form. The representative will provide information about programs, schedules, tuition and fees.

Since all instruction at SVPTI is in English, all applicants must demonstrate the ability to communicate in English. If there is sufficient doubt about the applicant's ability to communicate in English, a TOEFL (Test of English as a Foreign Language) test score result of at least 500 or higher will need to be documented by the applicant.

If an applicant tests below the 500 level on the TOEFL exam, or if they simply so choose, they will have the option to enroll in an ESL program at another institution at the appropriate level of instruction. Successful completion of the ESL Intermediate level program for such students will be required before they may enroll in any course at SVPTI.

It is anticipated that a basic knowledge of mathematics will be demonstrated through the Wonderlic Basic Skills Test, or preferably, through documentation of graduation from high school or possession of a GED Certificate.

Applicants will need basic familiarity with using computers as a prerequisite to taking any course.

SVPTI is committed to a policy of non-discrimination in admissions, and will not refuse service to any qualified individual based on color, sex, religion, or national origin.

Applicants will be advised that the use of color coding is one prominent method used as a standard in the industry for coding electronic components and drawings. Therefore, color-blind individuals may have difficulty in some courses.

Since SVPTI will not participate in any state or federal student loan programs, at least initially, it will be incumbent upon applicants to demonstrate the availability of sufficient financial sources to pay for their course of instruction. A registration fee of $100 must accompany the Application for Admission. The balance of tuition must be paid prior to the first session of instruction.

The signed enrollment agreement will not become effective until the prospective student attends the first class or session of instruction.

SVPTI will not offer or provide degree programs. All program offerings are Non-Degree or vocational in nature. Consequently, no postsecondary general education courses are required, nor will any be offered.

For all Non-Degree coursework, the Silicon Valley Polytechnic Institute will assess and evaluate student performance in order to grant a passing or failing grade. The Silicon Valley Polytechnic Institute will require that a student earn at least a C average (2 points on a 4 point scale) in order to satisfactorily complete a course of instruction.

As can be referenced in the course syllabi, a student must attain an earned average of no less than 60% to pass a course of instruction. For all Non-Degree coursework, SVPTI will assess and evaluate student performance in order to grant a grade of A, B, or C. SVPTI will require that a student earn at least a D average (1 point on a 4 point scale) in order to satisfactorily complete a course of instruction.

The basic grading standard will be:

| | |
|---|---|
| A | 90% - 100% |
| B | 80% - 89% |
| C | 70% - 79% |
| D | 60% - 69% |
| F | Below 60% |

Grades will be based on predominantly objective criteria such as exam results, projects, presentations, maintaining attendance, participation in class and engagement with the material.
SVPTI does not accept credits from other institutions, and has no articulation agreement with any other schools allowing the automatic acceptance of credit earned at any other institution.

**Scholastic Regulations:**

In order to maintain satisfactory progress as established by SVPTI, a student must maintain attendance (as explained below), perform satisfactorily throughout the program, and meet the minimum criteria established for completing the program.

**Attendance Policies:**

Students must maintain successful attendance. Each student is expected to attend every meeting of every class in which they are enrolled. Attendance will be recorded during each class.

Absenteeism may result in a warning, suspension, or dismissal. SVPTI will require a minimum attendance of at least 80% of all classes in order to complete a course. Individual instructors, however, can require a higher standard in their classes. Individual instructors will determine warning, suspension, and dismissal thresholds within this basic guideline.

Any work missed must be made-up within the basic policy for attendance set forth by the instructor. Individual instructor policies must operate within the SVPTI standard for attendance. Students are responsible for all make-up work as a result of any missed classes. It is the student's responsibility to contact the appropriate faculty member(s) concerning possible make-up work. Make-up work will be at the discretion of each instructor.

Students are expected to be present at the beginning of each class session. It will be the student's responsibility to inform that instructor after class if they arrive after attendance is recorded.

Absence of 21 consecutive days without notification will result in an assumption of student withdrawal.

**Dismissal and Suspension Policies:**

SVPTI reserves the right to suspend or terminate any student whose conduct is deemed inappropriate and disruptive to instruction. Such conduct includes: excessive absences or tardiness; failure to maintain satisfactory progress; inappropriate behavior toward another student or staff member; failure to abide by school rules and regulations; failure to meet financial obligations; any other conduct deemed sufficiently disruptive of instruction so that, in the estimation of the instructor and CEO/President, continued instruction is not a reasonable or constructive proposition.

Students who have been suspended or terminated may request reinstatement in writing to the CEO/President after a period of at least thirty days.

A student may request and be granted a Leave of Absence in exceptional circumstances wherein it is determined to be impossible or unlikely that the student will be able to maintain attendance or satisfactory progress for a given period of time. A Leave of Absence may be granted for sufficient cause by written petition to the instructor and/or CEO/President. The CEO/President will discuss the situation with the instructor, and, with benefit of the instructor's recommendation, authorize a Leave of Absence of no more than three months.

Any situation requiring a student absence or suspension longer than three months will necessitate the withdrawal of the student and any appropriate refunds.

**TARDINESS**

The Silicon Valley Polytechnic Institute is a serious training program designed to maximize every moment of instruction and interaction between student and instructor. The instructor takes the program of instruction very seriously, and it is expected that the student will do so as well. At the same time that students benefit from the highly individualized instruction, the success of the program as well as the student is dependent on maximizing the demanding skills learned and applied during the course of instruction.

Therefore, students will be permitted no more than three instances of excessive tardiness prior to being subject to dismissal from the program. Excessive tardiness is defined as more than three instances during the course of instruction when the student is more than 15 minutes late at either the commencement of the class in the morning or in the afternoon.

Students will receive a warning and reminder of this policy after each of the first three instances of excessive tardiness. The Silicon Valley Polytechnic Institute reserves the right to dismiss a student for excessive tardiness.

The instructor will determine what constitutes a valid excuse for tardiness. The general rule will be whether a reasonable person in similar circumstances would be in a position to arrive ready for instruction at the appointed time.

## DROPOUT AND LEAVE OF ABSENCE POLICY

Students may initially request orally or in writing to drop out of the program or to receive a grant of a leave of absence for sufficient reasons as determined by the instructor. If such a request is communicated orally, it shall be requested in writing prior to approval by the instructor. This will be for the purpose of documenting the student record.

Re-admission to the program will be at the sole discretion and under conditions determined as appropriate and necessary by the instructor. The primary governing factor for re-admission will be the passage of time since the student was last in the program, and the instructor's estimate of student progress and capability, and the satisfaction of financial requirements.

Under no conditions will a student be permitted a leave of absence for more than a three month period. If a student needs to discontinue the program of instruction for a period of more than three months, the student will receive a refund of paid tuition according to the refund policy and must thereafter be readmitted to the program.

Licensure is not required for these student graduates in order to work in the field and pursue their trade or vocation. SVPTI will not guarantee any employment or specific jobs upon completion of training. Instructors, in response to student questions, may offer general suggestions and references for locating employment in the field. However, SVPTI will make no representations about guaranteed or likely placement with an employer upon completion of any of its programs.

A very high percentage of students are typically already employed in the field in which they seek further training.

## WITHDRAWALS AND REFUNDS

You have the right to withdraw from a course of instruction at any time. It is preferred that a notice of withdrawal be made in writing to the address of the school shown on the first page of this Agreement. But please be advised that a constructive withdrawal of a student may also be made by the school. Such a withdrawal will be determined to have occurred, if in the estimation of the school and instructor, the student has missed more than 4 training sessions without any excuse and/or notification.

If a student wishes to withdraw from the institution or a course of instruction, the student must notify the school in writing. The request for termination should be send to SVPTI, 1762 Technology Drive, Suite 227, San Jose, CA 95110.

Any student has the right to cancel this enrollment agreement and obtain a refund of charges paid through attendance at the first class session, or the seventh day after enrollment, whichever is later.

Cancellation shall occur when you give written notice of cancellation at the address of the school shown on the top of the first page of the Enrollment Agreement. Please send the notice of cancellation addressed to SVPTI, 1762 Technology Drive, Suite 227, San Jose, CA 95110. If you cancel this Agreement, the school will refund any money that you paid, less any non-refundable charges and deduction for equipment not timely returned in good condition, within 45 days after your Notice of Cancellation is received.

## REFUND POLICY:

The institutional refund policy for students who have completed 60 percent or less of the course of instruction, and who have not cancelled as explained above, shall be a pro rata refund.

You are obligated to pay only for educational services received and for unreturned equipment. The refund shall be the amount you paid for instruction multiplied by a fraction, the numerator of which is the number of hours of instruction which you have not received but for which you have paid, and the denominator of which is the total number of hours of instruction for which you have paid.

If the amount you have paid is more than the amount that you owe for the time you attended, then a refund will be made within forty-five days of withdrawal. If the amount that you owe is more than the amount that you have already paid, then you will have to make arrangements to pay.

Students whose entire tuition and fees are paid by a third party organization are not eligible for a refund.

### Distance Education Refund Provisions:

An institution offering a distance educational program where the instruction is not offered in real time must transmit the first lesson and any materials to any student within seven days after the institution accepts the student for admission. The student has the right to cancel the agreement and receive a full refund as described above before the first lesson and materials are received. Cancellation is effective on the date written notice of cancellation is sent. If the institution sent the first lesson and materials before an

effective cancellation notice was received, the institution shall make a refund within 45 days after the student's return of the materials.

An institution must transmit all of the lessons and other materials to the student if the student has fully paid for the educational program, and after having received the first lesson and initial materials, requests in writing that all of the material be sent. If the institution transmits the balance of the material as the student requests, the institution must remain obligated to provide the other educational services it agreed to provide, such as responses to student inquiries, student and faculty interaction, and evaluation and comment on lessons submitted by the student, but shall not be obligated to pay any refund after all of the lessons and material are transmitted.

**Federal or State Loans:**

If a student has received federal student financial aid funds, the student is entitled to a refund of moneys not paid from federal student financial aid programs funds. If the student is eligible for a loan guaranteed by the federal or state government and the student defaults on the loan, both of the following may occur:

1. The federal or state government or a loan guarantee agency may take action against the student, including applying any income tax refund to which the person is entitled to reduce the balance owed on the loan.
2. The student may not be eligible for any other federal student financial aid at another institution or other government assistance until the loan is repaid.

## NOTICE CONCERNING TRANSFERABILITY OF CREDITS AND CREDENTIALS EARNED AT OUR INSTITUTION

The transferability of credits you earn at Silicon Valley Polytechnic Institute (SVPTI) is at the complete discretion of an institution to which you may seek to transfer. Acceptance of the units or degree is also at the complete discretion of the institution to which you may seek to transfer. If the certificate that you earn at this institution is not accepted at the institution to which you seek to transfer, you may be required to repeat some or all of your coursework at that institution.

For this reason you should make certain that your attendance at this institution will meet your educational goals. This may include contacting an institution to which you may seek to transfer after attending SVPTI to determine if your units or degree will transfer.

Prior to signing an enrollment agreement, you must be given a catalog or brochure and a School Performance Fact Sheet, which you are encouraged to review prior to signing this agreement. These documents contain important policies and performance data for this institution. This institution is required to have you sign and date the information included in the School Performance Fact Sheet relating to completion rates, placement rates, license examination passage rates, and salaries or wages, prior to signing this agreement.

It is important to note that SVPTI is a new institution. Therefore the facts stated immediately above are undetermined at this time, and it is not required to provide this information.

## PROBATION AND DISMISSAL

Silicon Valley Polytechnic Institute reserves the right to suspend or terminate any student whose conduct is deemed inappropriate and disruptive to instruction. Students will be expected to fully observe policies and rules of conduct of the Silicon Valley Polytechnic Institute. Such conduct includes: excessive absences or tardiness; failure to maintain satisfactory progress; inappropriate behavior toward another student or staff member; failure to abide by school rules and regulations; failure to meet financial obligations; any other conduct deemed sufficiently disruptive of instruction so that, in the estimation of the instructor and CEO/President, continued instruction is not a reasonable or constructive proposition.

Students who have been suspended or terminated may request reinstatement in writing to the CEO/President after a period of at least thirty days. Decisions on reinstatement will be at the sole discretion of Silicon Valley Polytechnic Institute.

## TOTAL CHARGES TO BE PAID UPON ENROLLMENT:

| | |
|---|---|
| Tuition | $3000 per course |
| Registration Fee | NA |
| STRF Fee | *NA |
| Leave of Absence Fee | N/A |
| Textbooks or Materials Charges | Student is responsible for purchasing necessary textbooks. Estimated charges: |

*After January 1 2015 schools shall discontinue collecting STRF assessments.

**The student will be responsible for these amounts. If the student has a student loan, they will be responsible for repaying the loan amount plus any interest, less the amount of any determined refund.**

***STUDENT TUITION RECOVERY FUND (STRF) FEES:**

*After January 1 2015 schools shall discontinue collecting STRF assessments.

## FEDERAL AND STATE FINANCIAL AID PROGRAMS

Silicon Valley Polytechnic Institute does not participate in any federal or state financial aid programs.

## STUDENT LOANS

Students are responsible for these amounts. If a student has a student loan, they are responsible for repaying the loan amount plus any interest, less the amount of any determined refund. If a student has received federal student financial aid funds, the student is entitled to a refund of the moneys not paid from federal student financial aid program funds.

## BANKRUPTCY

The State of California requires that we inform students whether Silicon Valley Polytechnic Institute has a pending petition in bankruptcy, is operating as a debtor in possession, or has filed a petition within the preceding five years that resulted in reorganization under Chapter 11 of the United States Bankruptcy Code. None of these circumstances has occurred.

## PLACEMENT SERVICES

SVPTI will not guarantee any employment or specific jobs upon completion of training. Instructors, in response to student questions, may offer general suggestions and references for locating employment in the field. However, SVPTI will make no representations about guaranteed or likely placement with an employer upon completion of any of its programs.

A very high percentage of students are typically already employed in the field in which they seek further training.

## FACILITIES AND EQUIPMENT

SVPTI training programs are class room based and students do not need any specific equipment. We will use computers, projectors, and white boards.

The proposed programs for SVPTI will be provided at its main location. SVPTI is located at 1762 Technology Drive, Suite 227, San Jose, CA 95110. The school premises are located on the second floor of a two story building in an office complex with ample parking.

The institution's floor plan shows two suites consisting of approximately 2543 square feet for Suite 227 and another 1030 square feet for Suite 228. The floor plan includes four classrooms, with the remaining space primarily shared between offices, a reception area, and administrative support functions, a conference room and library area, and kitchen facility. Restroom facilities are located in two nearby locations, one adjacent to Suite 227, and another down a hallway near Suite 228.

SVPTI is located in a pleasant office park with similar two-story buildings and a diversity of businesses appropriate to an office park. The overall appearance of the facility is that it is perhaps 10 to 15 years old with mature trees and landscaping. Offices and classrooms have plenty of windows. Rooms are ample in size. The facility is well-maintained and has an atmosphere conducive to learning.

## LIBRARY AND INFORMATION RESOURCES

All students are provided with the program or course text and software at no extra charge.

Students also have access to the Internet for any reference purpose through the various computers on-site.

Students do have access to an on-site reference library. Students will be provided with a letter of introduction if necessary by SVPTI for access to any other library facilities. However, between what is provided to students by SVPTI in terms of texts and software, and their access to the Internet, this is really all that is necessary for this type of instruction.

The proposed instruction will be provided with a very low ratio of instructors to students. Over the course of this type of instruction there is ample opportunity, actually much more opportunity than is typically the case, for direct exchange between the instructor and the student. A wealth of information is provided in this manner.

The library resources as described above are more than sufficient to support the instructional needs of anticipated or projected students.

## STUDENT SERVICES

Though Silicon Valley Polytechnic Institute does not provide actual tutorials, the training provided has a very favorable instructor-to-student ratio, thereby facilitating instruction and learning for students. Though this teaching method is not by itself considered to constitute a traditional “student service,” as a practical matter, it is far more valuable to the individual student than many other more traditional student services.

There is a considerable amount of “academic counseling” built into this program. Because the nature of the instruction is relatively intimate and direct, students will inevitably glean a considerable amount of practical and useful information from the instructor during the training, especially, of course, in the practical instructional phase.

Silicon Valley Polytechnic Institute carefully balances and integrates theory with practical content and processes in order to considerably shorten the student’s learning curve.

With the exception of required textbooks and writing materials, any required materials or equipment for practicum or other instruction are provided by the Silicon Valley Polytechnic Institute and paid for as part of the tuition.

Academic counseling is provided by or through instructors as well as the CEO/President on occasion.

There is a student lounge area with a refrigerator and microwave. Students may use this area to lunch, rest, or study.

A small library or reference area is provided. Some copies of texts as well as industry trade journals and magazines are available for browsing.

The above items are for student use during normal school hours only. There will be no lending library.

There is plenty of parking immediately adjacent to the building.

Silicon Valley Polytechnic Institute is conveniently accessible off a main thoroughfare and near a major freeway. A variety of retail services are available nearby.

## NEARBY HOUSING

Silicon Valley Polytechnic Institute has no dormitory facilities. The availability of housing nearby varies greatly in price and lease terms. Rentals range in price from moderate to expensive.

Silicon Valley Polytechnic Institute has no responsibility to find or assist students with their housing needs. This is the sole responsibility of the student.

## STUDENT VISAS

Silicon Valley Polytechnic Institute does not admit students with student visas from other countries.

## SCHOOL FINANCIAL AID

There is no private financing available through the school. Students are advised to obtain financial aid from a financial institution. Students at SVPTI are typically able to pay for a course of instruction upon enrollment.

## DISTANCE EDUCATION

No part of the required instruction taken through Silicon Valley Polytechnic Institute may be acquired via distance learning. Of course, some of the instruction may be supplemented via distance learning methods.

## STUDENT RIGHTS AND GRIEVANCES

Students at Silicon Valley Polytechnic Institute enjoy all the rights and privileges mentioned elsewhere in this catalog, including the right to cancel or withdraw, the right to a reasonable refund in such circumstances, and the privileges associated with being a student at the school.

However, it is recognized that, even with a favorable ratio of instructors to students, a dispute may arise with respect to the instruction or a school policy or practice that a student perceives as unfair or damaging.

A student may lodge a complaint orally or in writing to the instructor at the address of the school. The instructor, upon receipt of a complaint, will attempt to resolve the issue(s) directly with the student.

If the student complaint is not resolved within a reasonable period of time, for example within three to five days, or prior to the need for the student to lodge the complaint again, the instructor will advise the student that the complaint must be provided in writing if it hasn't been already. At that point, the instructor will provide the student with a written summary of the official complaint policy, as described in this catalog.

If a student complains in writing, the Silicon Valley Polytechnic Institute will provide the student with a written response within ten days of receipt of the student complaint. The written response will include a summary of the school investigation and disposition of the complaint. If the complaint or relief requested by the student is rejected, specific reasons will be given for the rejection.

If the student remains dissatisfied with the rejection or proposed remedy provided by the school, they may resort to contacting the Bureau at the address provided on their enrollment agreement or take other appropriate action as dictated by the circumstances.

## STUDENT RECORDS

SVPTI will maintain a file for each student who enrolls in the institution regardless of whether the student completes the educational service.

As set forth in California Education Code (CEC) §94900, Silicon Valley Polytechnic Institute (SVPTI) will maintain records with the name and most current address, e-mail address, and telephone number of each student enrolled in an educational program at the institution. Course and faculty information will be maintained as a matter of record for a period of not less than five years, and will contain the following information:

- Complete and accurate records of the educational programs offered and the curriculum for each
- The names and addresses of the members of the faculty, and
- Records of the educational qualifications of each member of the faculty.

In addition to the requirements of CEC Section 94900, the file shall contain all of the following applicable information per CCR Section 71920 :

- Written records and transcripts of any formal education or training, testing, or experience that are relevant to the student's qualifications for admission to the institution or the institution's award of credit or acceptance of transfer credits including the following:

  (A) Evidence of high school completion or equivalency or other documentation establishing the student's ability to do college level work;

  (B) Records documenting units of credit earned at other institutions that have been accepted and applied by the institution as transfer credits toward the student's completion of an educational program;

  (C) Grades or findings from any examination of academic ability or educational achievement used for admission or college placement purposes;

(D) All of the documents evidencing a student's prior experiential learning upon which the institution and the faculty base the award of any credit;

**Please note that since SVPTI does not offer any degree and/or credit, student's prior experiential learning will not be considered as a basis for acceptance and/or granting the certificate.**

- Personal information regarding a student's age, gender, and ethnicity if that information has been voluntarily supplied by the student;
- Copies of all documents signed by the student, including contracts, instruments of indebtedness, and documents relating to financial aid;
- Records of the dates of enrollment and, if applicable, withdrawal from the institution, leaves of absence, and graduation; and
- A transcript showing all of the following:

  (A) The classes and courses or other educational programs that were completed, or were attempted but not completed, and the dates of completion or withdrawal;

  (B) The final grades or evaluations given to the student;45

  (C) Credit awarded for prior experiential learning, including the course title for which credit was awarded and the amount of credit **(Please note this does not apply to SVPTI since as mentioned above, SVPTI will not consider student's prior experiential learning as a basis for acceptance and/or granting the certificate);**

  (D) Credit for courses earned at other institutions;

  (E) Credit based on any examination of academic ability or educational achievement used for admission or college placement purposes;

  (F) Degrees and diplomas awarded the student; and

  (G) The name, address, email address, and telephone number of the institution.

- For independent study courses, course outlines or learning contracts signed by the faculty and administrators who approved the course;
- The dissertations, theses, and other student projects submitted by graduate students;
- A copy of documents relating to student financial aid that are required to be maintained by law or by a loan guarantee agency;
- A document showing the total amount of money received from or on behalf of the student and the date or dates on which the money was received;
- A document specifying the amount of a refund, including the amount refunded for tuition and the amount for other itemized charges, the method of calculating the refund, the date the refund was made, and the name and address of the person or entity to which the refund was sent;
- Copies of any official advisory notices or warnings regarding the student's progress; and
- Complaints received from the student.

SVPTI will also keep the following documentation in the student record:

- The application for admission
- The notice or letter of acceptance or admission to the Institute
- Any documentation regarding cancellation, withdrawal, leave of absence, refund, or correspondence regarding a disciplinary action
- The title of the certificate granted to the student
- The date the certificate was granted
- The courses and units upon which the certificate was based (transcript)
- The grades earned in each course by the student (transcript)
- Any documentation regarding graduation
- Any correspondence regarding a student complaint
- Any calculation of a refund amount due to the student
- Any correspondence regarding any of the above.

Financial records will generally be maintained separate from academic documentation. These records will be maintained as hardcopies and also easily accessible and downloadable for the review of any authorized institutional officer or regulating authority.

All student records will be maintained in California. All student transcripts will be maintained and accessible to students for a period of not less than fifty years.

Finally, after a sufficient period of operation, and as required, SVPTI will maintain on-site for a period of not less than five years all data and records regarding completion, placement, licensure (if applicable), and salary disclosure requirements for graduates who find employment in the field within the guidelines prescribed in California Education Code Section 94928.

## OCCUPATIONS OR JOB TITLES

Silicon Valley Polytechnic Institute will not guarantee any employment or specific jobs upon completion of training. Instructors, in response to student questions, may offer general suggestions and references for locating employment in the field. However, Silicon Valley Polytechnic Institute will make no representations about guaranteed or likely placement with an employer upon completion of any of its programs.

A significant percentage of students may already be employed in some capacity in the field in which they seek further training.

There will be no formalized placement office at Silicon Valley Polytechnic Institute. But it is expected that Silicon Valley Polytechnic Institute will, especially as its reputation grows, have a considerable network of contacts within the local and regional business community and its particular business sector. Due to the nature of the instruction and the relatively close-knit community of a small to medium size school, it is further expected that fellow students, instructors, as well as school officials will be able to meaningfully assist students in their search for and ability to obtain employment in the sector.

Proximity to the populous counties of the Bay Area, of which Silicon Valley Polytechnic Institute will be a part, will materially assist these endeavors. However, it is important to remember that there are no specific occupations or job guarantees or promises of

placement made upon graduation from a Silicon Valley Polytechnic Institute course or program.

Sample SOC Codes for typical job classifications available to graduates are as follows:

| | |
|---|---|
| 17-3011 | Civil Computer-Aided Design and Drafting Technicians |
| 17-3011 | Civil Drafters |
| 15-1132 | Computer Applications Engineers |
| 51-4010 | Computer Control Programmers and Operators |
| 17-2061 | Computer Hardware Designers |
| 17-2061 | Computer Hardware Developers |
| 17-2060 | Computer Hardware Engineers |
| 17-2061 | Computer Hardware Engineers |
| 15-1131 | Computer Programmers |
| 49-2011 | Computer Repairers |
| 17-1012 | Landscape Architects |
| 47-2111 | Solar PV Electricians |
| 47-2231 | Solar PV Installers |
| 47-2111 | Solar Photovoltaic Electricians |
| 47-2230 | Solar Photovoltaic Installers |
| 47-2231 | Solar Photovoltaic Installers |
| 17-3012 | Technicians, Electrical Computer-Aided Design and Drafting |
| 17-3023 | Technicians, Electrical Design |
| 17-3023 | Technicians, Electrical Engineering |
| 17-3024 | Technicians, Electro-Mechanical |
| 17-3023 | Technicians, Electronics Engineering |

SVPTI prides itself on the attention and instruction provided to students. Students will obtain an understanding and appreciation for both the theory and practical knowledge of the subjects covered. You will find your pursuit of training at SVPTI enhanced by instructors who care and have direct experience with what they teach. And you will find that instruction supplemented by a learning environment conducive to obtaining what you need.

## APPENDIX –I

This appendix contains the detail description of all programs offered by SVPTI.

*a) Course Title:*

## Computer Aided Design and Drafting with AutoCAD (CAD-100)

*b) Objectives:*
AutoCAD Design and Drafting for Professionals provides students with extensive hands-on experience with the latest AutoCAD software, which is the world's leading CAD software for design & drafting. Participants will work with advanced drafting methods, as well as powerful AutoCAD features with exmaples in various aspects of design exploration for architectural, civil, mechanical, and electrical applications.

*d) Length of program:*
The course duration is 12 weeks.

*e) Class Sessions*
Classes are being held twice a week, with each session typically 3 hours long.

*f) Text Books*
*AutoCAD 2011, A Problem Solving Approach*, Sham Tickoo, autodesk Press.

*g) Course Outline*

- Why use 3D Surfaces vs. Solids
- Surfaces and Solids
- Creating surfaces
- Lines, arcs and circles with thickness
- 3D Faces
- 3D Mesh
- Creating solids
- Primitives
- Extrude
- Revolve
- Editing surfaces, solids
- Spherical & Cylindrical coordinate systems
- Co-ordinate Systems, Editing Tools
- World Co-ordinate System
- UCSICON
- UCS - how to set up efficiently
- Display Commands - dview, ddvpoint, plan, vpoint
- 3D Drawing and Editing Commands. Primitives
- Model Space/Paper Space
- Editing viewports
- Placing rendered images in a viewport
- Visualization Techniques
- Rendering Concepts
- Adding Materials to the Model
- Scenes and Lighting
- Adding Bitmap Images
- Class Exercises and projects

*h) Education Requirements*
High School or higher

*i) Course Level*
Entry Level, Technician

*j) Method of Instruction*
On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*
Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

**Advanced and 3D Computer Drafting and Design with AutoCAD (CAD-120)**

*b) Objectives:*

This course introduces students to the process, tools, and methodology of computer drafting with AutoCAD, the world's leading CAD software for design & drafting. This multipurpose class is intended for those who have little or no experience with AutoCAD. During the course, students will acquire basic skills in the use of AutoCAD software and design techniques toward various applications.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, with each session typically 3 hours long.

*f) Text Books*

*AutoCAD 2010, A Problem Solving Approach,* Sham Tickoo, autodesk Press.

*g) Course Outline*

- Getting Started with AutoCAD
- Basic Drawing and Editing Commands
- Drawing Organization and Information
- Organizing Your Drawing with Layers
- Advanced Editing Commands
- Inserting Blocks
- Printing
- Annotating
- Adding Text
- Hatching
- Adding Dimensions
- Advanced Editing Features
- Changing an Object's Length
- Productivity Tools
- Efficient Construction Techniques
- Accurate Positioning
- Creating and Managing Blocks
- Drawing Setup and Utilities
- Creating Templates
- Advanced Viewing Tools
- Quick Editing Techniques
- Viewing What You Need
- Advanced Object Types
- Polylines and Regions
- Multilines
- Advanced Blocks and Attributes
- Referencing and Sharing Information
- External Reference
- Working with Images
- Layouts and Plotting
- Working with Layouts
- Drawing Standards and System Setup
- Maintaining Standards
- CAD Standards
- Introduction to Customization

*h) Education Requirements*

High School or higher

*i) Course Level*

Entry Level, Technician

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

***a) Course Title:***

## Mechanical Drafting Fundamentals (CAD-130)

*b) Objectives:*

This course introduces fundamental concepts and operations necessary to utilize personal computer for developing fundamental drafting techniques. Emphasis is placed on the basic concepts, geometric terms/media sizes, and techniques necessary for CAD applications. Topics include history of drafting, safety practices, terminology, hardware and software care and use, basic entities, CAD commands, line relationships, basic CAD applications, and geometric construction.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, with each session typically 3 hours long.

*f) Text Books*

The Art of Mechanical Drawing: A Practical Course for Drafting and Design
William F. Willard

*g) Course Outline*

- Describe the role of technical graphics in the engineering design process.
- Produce multi-view orthographic views.
- Create sectional views.
- Create auxiliary views.
- Scale drawings.
- Apply dimensions to drawings.
- Create pictorial drawings.
- Prepare development drawings.
- Identify graphics for fastening and finishing machine components.

*h) Education Requirements*

High School or higher

*i) Course Level*

Entry Level, Technician

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

***a) Course Title:***

## 3D Computer Aided Design and Drafting with SolidWorks (CAD-140)

*b) Objectives:*

This course introduces the students to the process, tools, and methodology of 3D computer drafting with SolidWorks, the world's leading CAD software for 3D design & drafting and modeling. During the course, the students will acquire skills in the use of SolidWorks software and design techniques for design and drawing of various 3D structures for many diverse applications. This course prepares students for entry-level to mid-level positions in the industry.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, with each session typically 3 hours long.

*f) Text Books*

SolidWorks 2010 for Designers, By Sham Tickoo, Purdue University, ISBN: 1-932709-26-6

*g) Course Outline*

- Why use 3D Surfaces vs. Solids
- Surfaces and Solids
- Creating surfaces
- Lines, arcs and circles with thickness
- 3D Faces
- 3D Mesh
- Creating solids
- Primitives
- Extrude
- Revolve
- Editing surfaces, solids
- Spherical & Cylindrical coordinate systems
- Co-ordinate Systems, Editing Tools
- World Co-ordinate System
- UCSICON
- UCS - how to set up efficiently
- Display Commands - dview, ddvpoint, plan, vpoint
- 3D Drawing and Editing Commands. Primitives
- Model Space/Paper Space
- Editing viewports
- Placing rendered images in a viewport
- Visualization Techniques
- Rendering Concepts
- Adding Materials to the Model
- Scenes and Lighting
- Adding Bitmap Images
- Class Exercises and projects

*h) Education Requirements*

High School or higher

*i) Course Level*

Entry Level, Technician

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

***a) Course Title:***

## Advanced 3D Computer Aided Design and Drafting with SolidWorks (CAD-160)

### *b) Objectives:*

This course introduces the students to the advanced modeling techniques using SolidWorks, the authoritarian in 3D Mechanical Computer Aided Design (MCAD). This multipurpose class is designed for students that have completed the introductory class to SolidWorks, or individuals with industry experience looking to expand their knowledge with SolidWorks. Thru various examples, students will utilize SolidWorks software to learn advanced design techniques geared toward mechanical, structural, and architectural applications. This course prepares students for mid-level to advanced-level positions in the industry.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, with each session typically 3 hours long.

*f) Text Books*

SolidWorks 2010 for Designers, By Sham Tickoo, Purdue University, ISBN: 1-932709-26-6

*g) Course Outline*

- Advanced sketching techniques
- 3D Sketching
- Auto dimension
- Contrain all/find equal
- 2D to 3D Tools
- Sweeps and Lofts
- Surfacing Tools
- Sheet metal Tools
- Design Library
- Troubleshooting parts (fixing rebuild errors)
- Disjoint bodies/multibody part mode1ing
- Weldment Tools
- Configurations & Design Tables
- Importing/Exporting files
- Advanced assembly techniques
- Advanced mates
- Assembly level features
- Patterns and mirrors
- Flexible Assemblies
- Top Down Assembly modeling
- Layout Sketches
- Collision Detection and Physical Dynamics
- Large Assembly modeling techniques
- Assembly Configurations & Design Tables

### *h) Education Requirements*

High School or higher

### *i) Course Level*

Entry Level, Technician

### *j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

### k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## Autodesk Revit Architecture Essentials (CAD-180)

*b) Objectives:*

This course introduces the students to the process, tools, and methodology of using Autodesk Revit for architectural drafting. This course is intended for those who have already taken the AutoCAD or are fairly familiar with AutoCAD. During the course, the students will acquire skills in the use of Revit software and design techniques for various architectural applications.

*d) Length of program:*

The course duration is 12 weeks long.

*e) Class Sessions*

Classes are being held twice a week, with each session typically 3 hours long.

*f) Text Books*

Mastering Autodesk Revit Architecture 2011, By Eddy Krygiel, *et al*
ISBN-10: 0470626968

*g) Course Outline*

- What Is Revit Architecture?
- Overview of the Revit Architecture Interface
- Revit Architecture File Types
- Creating Basic Floor Plans
- General Drawing and Sketch Tools
- Drawing Walls
- Adding Doors and Windows
- Setting Up Levels and Grids
- Creating and Using Levels
- Creating Structural Grids and Columns
- Modifying Specific Objects
- Selecting & Modifying Objects
- Modifying Walls
- Modifying Levels
- Modifying Doors and Windows
- Modifying Structural Grids and Columns
- Editing Commands
- Moving and Copying Objects
- Rotating Objects
- Resizing Objects
- Creating Linear and Radial Arrays
- Mirroring Objects
- Aligning Objects
- Splitting Walls and Lines
- Offsetting Objects
- Trimming and Extending
- Creating Views of the Model
- Using the Project Browser
- Working with Views
- Setting Up Views
- Viewing Elevations
- Cutting Sections
- Creating Callouts
- Duplicating Views
- Creating 3D Views
- Adding Components
- Loading Families from Libraries
- Manipulating Components
- Floors and Ceilings
- Creating Floors
- Creating Ceilings
- Creating Roofs
- Creating Roofs by Extrusion
- Stairs, Railings, and Ramps
- Creating Stairs
- Adding and Modifying Railings
- Creating Ramps
- Curtain Walls
- Creating Curtain Walls
- Creating Curtain Wall Types with Automatic
- Working with Curtain Wall Panels
- Attaching Mullions to Curtain Grids
- Sheets and Printing
- Setting Up Sheets
- Views and Sheets
- Printing Sheets
- Annotation
- Working With Text
- Adding Dimensions
- Adding Tags
- Building Schedules
- Detailing in Revit Architecture
- Setting Up Detail Views
- Creating Details
- Annotating Details
- Revision Tracking
- Creating Legen

*h) Education Requirements*

High School or higher

*i) Course Level*

Entry Level, Technician

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

**Computer and Network Security Essentials (CIE-150)**

*b) Objectives:*

This course introduces the students to Principles, mechanisms and implementation of computer security and data protection. Policy, encryption and authentication, access control and integrity models and mechanisms; network security; secure systems; programming and vulnerabilities analysis. The course will also include study of existing operating systems. This course prepares students for entry-level to mid-level positions in the industry.

*d) Length of program:*

The course duration is 12 weeks long.

*e) Class Sessions*

Classes are being held twice a week, with each session typically 3 hours long.

*f) Text Books*

Network Security Bible, By Eric Cole, ISBN: 0764573977

*g) Course Outline*

- What is computer security: notion of an informal policy, formalization of policy
- Encryption: classical, public-key; implementation, problems; the Linux file encryption mechanism and its cryptanalysis; the DES and RSA
- Authentication: model of authentication systems, traditional passwords, challenge/response, one-time passwords; cryptographic protocols, simple cryptosystems; the standard Linux authentication system, its limits and alternate forms; implementations of other mechanisms
- Access control: controlling access to resources, access matrix model, undecidability result, access control lists and capability lists; mandatory controls, originator controls; variants; Linux scheme and augmentations
- Integrity: cryptographic checksums, malicious logic, viruses, Trojan horses; defenses, prevention; Linus integrity checking tools and how they work; malicious logic and Linux
- Security-oriented programming: design principles, focusing on common problems; gates vs. privileged servers; environment, exception handling; writing secure servers and secure setuid/setgid programs in the Linux environment
- Networks and security: Internet Security Architecture, analysis of Internet protocols, design and implementation considerations; firewalls; Linux networking and security
- Penetration analysis: common types of flaws, examples, flaw hypothesis methodology, analysis of programs and systems; Linux instances of problems, flaws, and how to fix them
- Secure systems: types, models, design, changes to non-secure systems; comparative analysis

*h) Education Requirements*

*AA or higher*

*i) Course Level*

*Entry Level, Technician, Engineering*

*j) Method of Instruction*

*On Campus, combinations of lecture and hand-on computer lab*

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## Software Quality Assurance Essentials (CS-150)

*b) Objectives:*

This course focuses on techniques for ensuring software quality. In this course quality assurance is viewed as a holistic activity that runs through the entire development process: understanding the needs of clients and users; analyzing and documenting requirements; verifying and validating solutions through testing.

*d) Length of program:*

The course duration is 12 weeks long.

*e) Class Sessions*

Classes are being held twice a week, with each session typically 3 hours long.

*f) Text Books*

Software Quality Assurance, By D. Galin
ISBN 978-0-201-70945-2

*g) Course Outline*

- Evaluating usability of a software product.
- Requirements analysis. Software development as problem solving.
- Identifying, structuring, and classifying problems through Problem Frames.
- Building specifications from requirements.
- Verification and validation. Defining the testing mission. Test strategies.
- Techniques of conformance testing.
- Validating preliminary designs through prototyping.
- Quality management. Measuring software quality.
- Software quality standards.

*h) Education Requirements*
*AA or higher*

*i) Course Level*
*Entry Level, Technician, Engineering*

*j) Method of Instruction*
*On Campus, combinations of lecture and hand-on computer lab*

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## Solar Photovoltaic System Design Essentials (EN-100)

*b) Objectives:*

This course provides the students with a comprehensive understanding of Photovoltaic (PV) Solar systems. The class covers essentials of PV theory, design, configuration and installation techniques and employs a balanced combination of lecture and hands-on practice. The course is intended for contractors, installation consultants, and electricians new to the solar industry, and is intended to prepare participants for employment in renewable energy industry. This course prepares students for entry-level to mid-level positions in the industry.

*d) Length of program:*

The course duration is 12 weeks long.

*e) Class Sessions*

Classes are being held twice a week, with each session typically 3 hours long.

*f) Text Books*

Photovoltaic Systems, ATP Publications, ISBN 978-0-8269-1287-9

*g) Course Outline*

- Photovoltaics, photovoltaic (PV) system, and load.
- Advantages of using PV systems.
- Disadvantages of using PV systems.
- Process of electricity distribution.
- Development of PV technology.
- Common applications of PV systems.
- Common methods of converting solar radiation into heat energy.
- How solar energy can be harnessed through chemical processes.
- Characteristics and advantages of solar lighting.
- Solar radiation, solar irradiance, and the inverse square law.
- Solar irradiation.
- Solar constant and the solar spectrum in relation to extraterrestrial solar radiation.
- Characteristics of direct radiation and diffuse radiation.
- Various stages of Earth's orbit.
- Characteristics of solar time as contrasted with standard time.
- Various positions of the sun.
- Ways that array orientation can vary due to geographical and seasonal variations of the sun's path.
- Function of solar radiation data sets and which agencies provide the data.
- Customer concerns and site issues that may arise during a preliminary assessment.
  Common types of equipment needed to conduct site surveys.
- Features of the profile angle shading analysis method and the photographic method.
- Main reasons to consider accessibility when conducting a site survey.
- Factors to consider when evaluating roofs.
- Conducting an electrical assessment.
- Energy audit and opportunities for conservation and energy efficiency.
- Preparing a proposal.
- Major components of PV systems
- Common sources of electricity.
- Utility-interactive system and common metering arrangements.
- Advantages and classifications of hybrid systems.
- Basic composition and use of PV cells.
- Photovoltaic effect and the fundamentals of PV cells.
- Common PV cell materials.
- Advantages and disadvantages of different silicon wafers.
- Process of cell fabrication.
- How a PV device responds to changes in solar irradiance and temperature.
- Basic function and construction of modules and arrays.
- Function and main features of bypass diodes.
- Common module and array standards and performance ratings.
- Main principles and components of battery design.
- Steady-state and capacity.

*h) Education Requirements*

High School or higher

*i) Course Level*

Entry Level, Technician

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

**Advanced Solar Photovoltaic System Design (EN-120)**

*b) Objectives:*
This course provides the students with advanced topics in Photovoltaic (PV) Solar systems. The course is intended for contractors, installation consultants, and electricians new to the solar industry, and is intended to prepare participants for employment in renewable energy industry. This course prepares students for entry-level to mid-level positions in the industry.

*d) Length of program:*
The course duration is 12 weeks long.

*e) Class Sessions*
Classes are being held twice a week, with each session typically 3 hours long.

*f) Text Books*
Photovoltaic Systems, ATP Publications
ISBN 978-0-8269-1287-9

*g) Course Outline*

- Distributed generation and function of generators in an electric utility system.
- How inverters differ from generators.
- Main advantages of bimodal systems.
- Requirements associated with different points of connection.
- Compare and contrast the main methods of metering electricity.
- How legislation has impacted the adoption of PV and other distributed-power systems.
- Main procedural steps necessary for getting approval for an interconnection agreement.
- Common requirements of utility interconnection agreements.
- Role of building codes in electrical installations.
- Issues related to electrical contractor licensing.
- Building regulations that may restrict or facilitate construction
- Minimum requirements for most permit applications.
- Roles of permit fees and the plans review as requirements for permit issuance.
- Documentation commonly used during the inspection process.
- Common items included on an inspection check.
  Advantages and limitations of an inspection check.
- Steps involved in commissioning a new PV system.
- Maintenance tasks for arrays.
- Tasks and tools related to battery maintenance.
- Tasks performed for electrical equipment maintenance.
- Function of maintenance plans and maintenance logs.
  Steps involved in troubleshooting PV systems

*h) Education Requirements*
High School or higher

*i) Course Level*
Entry Level, Technician

*j) Method of Instruction*
On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*
Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

**Advanced Semiconductor Devices - Physics & TCAD (SS-200)**

*b) Objectives:*

This course introduces students to the physics, operations and applications of semiconductor devices such as PN and Schottky diodes, bipolar and CMOS transistors. TCAD software is used when necessary to enhance the learning experience.

*d) Length of program:*

The course duration is 12 weeks long.

*e) Class Sessions*

Classes are being held twice a week, with each session typically 3 hours long.

*f) Text Books*

Physics of Semiconductor Devices by S.M.Sze, Wiley Publication
SBN 471 84290 7

*g) Course Outline*

- Semiconductor Materials & Atomic Models
- Energy Bands and Charge Carriers
- Bond and Band Models
- Carrier Concentrations
- Drift and Diffusion
- Continuity Equations
- PN Juncti ons Chapter
- Abrupt Junction
- Linearly Graded Junction
- Continuity Equations
- Generation and Recombination
- I-V Characteristics
- Bipolar Transistor
- Ebers-Moll Model
- Second Order Effects
- MOS Structure
- Flat Band Model
- Non-Flat Band Model
- Interface Charge Effects
- MOS Field Effect Transistors
- MOSFET Parameters

*h) Education Requirements*

BSEE or higher

*i) Course Level*

Entry Level, Engineering

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

**Solar Photovoltaic Device Physics (SS-210)**

*b) Objectives:*

This course provides the students with a comprehensive understanding of the physics of solar cell. Course starts with a description of property of semiconducting materials such as Si, and GaAs and then gives a detail description of the physics of PN junction as related to PV. TCAD software is used extensively to enhance the student's learning experience. This course prepares students for entry-level to mid-level positions in the industry.

*d) Length of program:*

The course duration is 12 weeks long.

*e) Class Sessions*

Classes are being held twice a week, with each session typically 3 hours long.

*f) Text Books*

The Physics of Solar Cells, by Jenny Nelson
ISBN 1860943497

*g) Course Outline*

- Introduction to solar cells
- Brief comparison with other renewables
- Properties of sunlight
- p-n junction physics; operation of solar cells
- Cell characterization: I-V curve under dark and illumination conditions,
- cell efficiency, fill factor, short-circuit current, open-
- circuit voltage
- PV technologies:
- Single crystalline Si cells
- Micro-, poly-, and multi-crystalline Si cells
- Amorphous Si cells
- III-V multijunction cells
- Concentrator PV
- CIGS solar cells
- CdTe solar cells
- Dye-sensitized solar cells
- Organic solar cells
- Nanotechnology and solar cells
- Module manufacturing
- PV Economics

*h) Education Requirements*

BSEE or higher

*i) Course Level*

Entry Level, Engineering

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

**Advanced Semiconductor Technology and Fabrication (SS-220)**

*b) Objectives:*

This course introduces students to the technology and manufacturing of silicon microchips. Course starts with an overview of semiconductor technology and proceeds to offer a detail description of all the process steps and equipments for making the modern semiconductor devices/products. The course will also provide an overview description of the latest advancements in semiconductor technology.

*d) Length of program:*

The course duration is 12 weeks long.

*e) Class Sessions*

Classes are being held twice a week, with each session typically 3 hours long.

*f) Text Books*

Microchip Manufacturing, by S. Wolf, Lattice press
ISBN: 0-961672-8-8

*g) Course Outline*

- Introduction/Review of symbols, terminology, and notation of Semiconductor Process Technology.
- ITRS/Moore's law
- Overview of process technology, and fabrication steps.
- The PN junction, device physics/carrier concentrations and related equations.
- The MOS transistor and it's 4-terminal operation/related equations. Properties of MOS capacitors, and resistors.
- Design of Wafer Fabrication Process flows
- Wafer Fab equipment understanding
- Process Modeling thru Supreme programs
- Understanding Process Cross sections. SEM/doping profiles
- Relation between process parameters and electrical parameters.
- Cost model/Economics of wafer fabrication
- Safety issues involve in Semiconductor process steps.
- Wafer Fabrication facility design
- Post CMOS devices

*h) Education Requirements*

High School or higher

*i) Course Level*

Entry Level, Technician

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

***a) Course Title:***

## Applied Electricity and Electronics Fundamentals (EE-100)

*b) Objectives:*
This course introduces the students to the exciting world of electricity and electronics through theory and practice. By using several hands-on projects students learn basic to advanced principles behind the working of ubiquitous electrical and electronic circuits.

*d) Length of program:*
The course duration is 12 weeks.

*e) Class Sessions*
Classes are being held twice a week, typically 3 hours each.

*f) Text Books*
Electronic Circuit Fundamentals, Floyd, Prentice Hall

*g) Course Outline*

- Concepts of Work, Power and Energy
- Principles of Electricity
- Concepts of Electric Circuits
- Electric Circuit Components
- Dc Circuits
- Series Circuits
- Parallel Circuits
- Combination Circuits
- Voltage Divider Circuits
- Bridge Circuits
- Calculate Conductor Resistance
- Three-Wire (Edison) Circuits
- Principles of Electromagnetism
- Reading and Interpreting Electrical Drawings
- Electrical Code and Wiring
- AC Fundamentals
- Trigonometry in Electrical Calculations
- Using Vectors in Electrical Calculations
- Principles of Alternating Current
- Single-Phase Ac Circuits
- Principles of Inductance
- Principles of Capacitance
- Effects of Inductive Reactance
- Effects of Capacitive Reactance
- Circuit Protection Devices
- Circuit Protection Devices
- Transformer Fundamentals
- Voltage Regulation
- Lighting Fundamentals
- Incandescent Lighting Circuits
- Fluorescent Lighting Circuits
- Introduction to Electronics
- Transistors, Didoes, Thyristor
- Transistor Circuits
- Introduction to Digital Logic
- Op-Amp Circuits
- Basic Computer Hardware and Software
- Basic Computer Operating Systems and Networks
- Digital Logic Circuits

*h) Education Requirements*
High School or higher

*i) Course Level*
Entry Level, Technician

*j) Method of Instruction*
On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*
Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

***a) Course Title:***

## National Electrical Code (NEC) Training (EE-110)

*b) Objectives:*

This course is intended to explain the requirements of the National Electrical Code® and provides basic instruction on the newest editions. It discusses rules to minimize risk of electricity as a source of electric shock and as an ignition source of fire. The course further clarifies and refines student's grasp of grounding.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

NFPA 70 2011 National Electrical Code

*g) Course Outline*

- Use and Identification of Grounded Conductors Branch Circuits
- Feeders
- Branch-Circuit, Feeder and Service
- Calculations Outside Branch Circuits and Feeders
- Services
- Overcurrent Protection
- Grounding
- Transient Voltage Surge Suppressors
- Wiring Methods
- Conductors for General Wiring
- Cabinets, Cutout Boxes, Meter Socket Enclosures Outlet, Device, Pull, and Junction Boxes; Conduit Bodies; Fittings; and Manholes Armored Cable: Type AC
- Nonmetallic-Sheathed Cable: Types NM, NMC and NMS
- Flexible Metal Conduit: Type FMC
- Liquidtight Flexible Metal Conduit: Type LFMC Rigid Nonmetallic Conduit: Type RNC
- Liquidtight Flexible Nonmetallic Conduit: Type LFNC Electrical Nonmetallic Tubing: Type ENT
- Auxiliary Gutters
- Cablebus
- Metal Wireways
- Busways
- Surface Metal Raceways
- Surface Nonmetallic Raceways
- Cable Trays Flexible Cords and Cables
- Fixture Wires
- Switches
- Receptacles, Cord Connectors, and Attachment Caps Switchboards and Panelboards
- Luminaries, Lamp holders, Lamps
- Appliances
- Fixed Electric Space-Heating Equipment
- Motors, Motor Circuits, and Controllers, including Disconnecting Means for Motors
- Air Conditioning and Refrigeration Equipment Transformers and Transformer Vaults
- Equipment over 600 Volts, Nominal Special Occupancies
- Special Equipment
- Special Conditions
- Communication Systems

*h) Education Requirements*

High School or higher

*i) Course Level*

Entry Level, Technician

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

***a) Course Title:***

## Digital Logic Design Fundamentals (EE-120)

*b) Objectives:*

The course provides a modern introduction to logic design and the basic building blocks used in digital systems. The course starts with a discussion of combinational logic including logic gates, minimization techniques, arithmetic circuits and modern logic devices such as field programmable logic gates. The second part deals with sequential circuits: flip-flops, synthesis of sequential circuits, case studies including counters, registers, random access memories. State machines will be discussed next and illustrated through case studies of more complex systems using programmable logic devices. Different representations including truth table, logic gate, timing diagram, switch representation, state diagram, algorithmic state machine (ASM) chart will be discussed.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

Logic and Computer Design Fundamentals, by M. Mano and C. Kime, Prentice Hall
ISBN# 0138134006

*g) Course Outline*

- Principles of Boolean Algebra to manipulate and minimize logic expressions
- Use of K-maps to minimize and optimize two-level logic functions up to 5 variables
- Operation of latches, flip-flops, counters, registers, and register transfers
- Analyze the operation of sequential circuits using built with various flip-flops
- Concepts of data paths, control units and micro-operations and building block of digital systems

*h) Education Requirements*
*AA or higher*

*i) Course Level*
*Entry Level, Technician, Engineering*

*j) Method of Instruction*
*On Campus, combinations of lecture and hand-on computer lab*

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

***a) Course Title:***

## MATLAB for Engineering and Scientific Applications (EE-130)

*b) Objectives:*

This course is designed around learning MATLAB and applying it to a variety of engineering and scientific/research problems. The essentials of MATLAB are taught. These lessons are combined with instructions on fundamental simulation techniques and concepts. The objective of this course is to acquaint students with the basic tools as well as some of the techniques needed to use MATLAB software properly for solving many challenging projects.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

This course has no text book. Course workbook will be provided to students by the school.

*g) Course Outline*

- Brief history of Matlab
- Introduction to matlab desktop and programming environment
- A few basic commands
- Arithmetic operations
- Data structures in MATLAB, entering data into MATLAB
- Generating arrays and matrices
- Array and matrix indexing and operations
- Matrix algebra vs. element-by-element operations
- Linear Algebra and Eigenvalue Problems
- Root Finding
- Curve Fitting to Measured Data
- Logical operations (AND, OR, XOR,…)
- MATLAB commands
- MATLAB built-in functions
- Plotting in Matlab: 2D & 3D plots , colorbar and colormap
- Symbolic Manipulation in MATLAB
- MatLab I/O
- MATLAB sound capabilities
- MATLAB scripts (M-files)
- MATLAB Programming: Loop constructs & Conditional statements (if, elseif, while, break, etc.)
- MATLAB functions
- MATLAB Toolboxes

*h) Education Requirements*
*AA or higher*

*i) Course Level*
*Entry Level, Technician, Engineering*

*j) Method of Instruction*
*On Campus, combinations of lecture and hand-on computer lab*

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## IC Layout Design (EE-150)

*b) Objectives:*

One of the best training courses available in industry, this course introduces the students to the process, tools and methodology of IC Layout Design using the latest Design Automation tools. The course provides the students with the insight into the exciting field of semiconductor technology and electronic devices, and trains them in IC layout techniques for a variety of application in Digital, Analog, and RFIC. This training program prepares students for entry-level positions in the industry.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

This course has no text book. Course workbook will be provided to students by the school.

*g) Course Outline*

- Basic Electricity
- Basic Electronics
- Materials properties
- Conductors, Insulators, and Semiconductors
- Electronic Devices
- Resistors
- Transistors
- Diodes
- Capacitors
- Inductors
- Semiconductor processing
- Design Process Overview
- Electronic Circuits
- Analog, Digital, Mixed Signals
- Logic Gates
- Standard Cells
- Gate Arrays
- ASIC Design Methodology
- Standard Cell Library Design
- Diffusion Merging
- Combinational and Sequential Logic
- Floor Planning
- Power Grids
- IO Cells
- Latchup theory & prevention
- ESD Devices
- IC Layout Techniques
- Memory Layout Issues
- Bonding pad, Seal-ring, Scribe-line layout techniques.
- Power bus routing, bus slotting, and Clock net routing techniques
- Unix Training
- UNIX vi editor

*h) Education Requirements*

*High school or higher*

*i) Course Level*

*Entry Level, Technician, Engineering*

*j) Method of Instruction*

*On Campus, combinations of lecture and hand-on computer lab*

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## IC Layout Verification (EE-160)

*b) Objectives:*

This is an advanced hands-on course in the layout and verification of integrated circuits. Students study advanced design layout methods and employ specialized CAD tools to layout and verify circuits. This Layout Verification course is designed to show the students the fundamentals and essentials of DRC, LVS for those who have basic layout background.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

This course has no text book. Course workbook will be provided to students by the school.

*g) Course Outline*

- Design Flow
- Layout verification flow
- Boolean Operations
- Review of Design Rules
- DRC Flow
- DRC Rule File Creation
- Antenna Effects
- Density Check
- Identify DRC Errors
- LVS Rule File Creation
- Identify and Fix LVS Errors
- Various Hands-on Projects

*h) Education Requirements*

*AA or higher*

*i) Course Level*

*Entry Level, Technician, Engineering*

*j) Method of Instruction*

*On Campus, combinations of lecture and hand-on computer lab*

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## MEMS Design & Technology Fundamentals (EE-170)

*b) Objectives:*

This is an advanced hands-on course in the layout and verification of integrated circuits. Students study advanced design layout methods and employ specialized CAD tools to layout and verify circuits. This Layout Verification course is designed to show the students the fundamentals and essentials of DRC, LVS for those who have basic layout background.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

MEMS & Microsystems Design and Manufacture", by Tai-Ran Hsu

*g) Course Outline*

- Introduction to MEMS design
- Introduction to MOS Technology: Basic MOS Circuit, MOS Circuit Design
- MOS fabrication process: NMOS mask layout and L-Edit software
- MOSIS foundry service
- Integrated CMOS/MEMS Devices: A CMOS Thermal Isolated Gas Flow Sensor
- Micro Hot Wire
- CMOS Fabricated Micromechanical Structures
- Introduction to Accelerometer
- Accelerometer design based on MOSIS rules
- Bulk micro-machined accelerometer: static, dynamic, sensor system and fabrication
- MUMPS Foundry Services: Micro motor design
- Electrostatic micro actuator: Comb drive design
- Magnetic actuator
- Thermal actuator
- Piezoelectric actuator
- Shape memory alloy actuator
- Pneumatic actuator
- Term project presentation

*h) Education Requirements*

*AA or higher*

*i) Course Level*

*Entry Level, Technician, Engineering*

*j) Method of Instruction*

*On Campus, combinations of lecture and hand-on computer lab*

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## PCB and PWB Technology Fundamentals (EE-180)

*b) Objectives:*

This course explores fundamentals of PCB and PWB technologies, applications, design, and test. During the course students are introduced to the application of printed circuit board, materials properties, manufacturing techniques, components; surface mount and through hole, and general design & test methodologies, etc.. The course prepares the students for more advanced programs in PCB design.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

Clyde F. Coombs Jr., "COOMBS' PRINTED CIRCUITS HANDBOOK", McGraw-Hill Professional

*g) Course Outline*

- Connectivity
- Types of boards
  - Single sided
  - Double Sided
  - Multilayer PCB
- Surface Mount components
- General Design Considerations
- Mechanical Design Factors
- Board Size and Shapes
- Material Selection
- Electrical Design Factors
- Environmental Factors
- Layout Standards
- Base Materials
- Circuit Components and Hardware
- Fabrication Process
- Image Transfer
- Plating
- Etching
- Bare Board Testing
- Assembly
- Test in Assembly
- Multilayer Materials
- Flexible Circuits

*h) Education Requirements*

*AA or higher*

*i) Course Level*

*Entry Level, Technician, Engineering*

*j) Method of Instruction*

*On Campus, combinations of lecture and hand-on computer lab*

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

# PCB Layout Design (EE-185)

*b) Objectives:*

This course introduces students to the process, tools, and methodology of the PCB layout design. During the course students will develop basic skills in the use of the modern PCB layout design software and techniques. Schematics, printed circuit board layouts, symbols, and wiring diagrams will be produced on CAD workstation; terminology and the manufacturing process of printed circuit boards will be covered. The course prepares the students for the entry-level PCB layout position.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

Required: None

*g) Course Outline*

- Design Process Overview
- Common User Interface
- Invoking PCB Tools
- Design Creation Terminology
- Design Hierarchy
- Opening Down into a Component
- Process for Preparing a Schematic
- Placing Symbols on the Schematic Sheet
- Adding Wires
- Adding Properties
- Extracting Information from the Design
- Checking and Saving the Design
- Basic Geometry Types
- Display Layers
- Library Management
- Default Directory Hierarchy
- Saving Geometries
- Creating New Geometries
- Attributes
- Adding Geometry Pins
- Checking Geometries
- Introduction to Design Rules
- Mapping Files
- Creating a Part Number
- Checking Part Number Data
- Back Annotation
- Display Controls
- Component Labels
- Setting Display Attributes
- Component Height
- Placement Regions
- Interactive Placement - by Reference, by Connectivity, from Schematic
- Moving and Rotating Components
- Protecting and Fixing Components
- Mapping Components
- Using Board Station RE Placement
- Design Rules
- Physical Layers
- Rules for Pins and Vias
- Understanding Blind Pins and Blind/Buried Vias
- Routing Design Rules by Net and Layer
- NET_TYPE Property
- Interactive Routing
- Protecting Routing
- Area Fills
- Area Fill Connectivity
- Creating an Area Fill
- Changing Reference Designators
- The Artwork Order
- The Aperture Table
- Creating Artwork Data
- Opening Artwork Data
- Simulating Artwork Data
- The Drill Table
- Drill Data file
- Assigning Drill Symbols to Drill Sizes
- Simulating Drilling
- Drafting and Reports
- Creating a Fabrication Drawing
- Creating an Assembly Drawing
- Basic Drafting
- Adding Dimensions
- Dimensioning Styles
- Manufacturing Reports

*h) Education Requirements*
*AA or higher*

*i) Course Level*
*Entry Level, Technician, Engineering*

*j) Method of Instruction*
*On Campus, combinations of lecture and hand-on computer lab*

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## Advanced PCB Layout Design (EE-187)

*b) Objectives:*

This course introduces students to the advanced topics in PCB layout design. The course will allow students to become familiar with signal integrity analysis at the board level. It addresses transmission lines and their effects on digital circuitry and printed circuit boards. The course will present detailed examples from real-world designs to demonstrate the necessity of understanding signal integrity issues and applying sound signal integrity principles to PCB Design. The course is developed around advanced design methodology and prepares the students for the entry-level PCB layout position.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

Required: None

*g) Course Outline*

- Transmission lines and their effect on digital circuitry
- Printed circuit boards: drivers, receivers, Zo, Zdiff, stack up
- Quality board designs
- Termination, topology, timing, parasitics, etc
- Crosstalk: understanding and preventing
- Differential pair: termination, routing, timing, EMI
- Clock distribution, high speed busses, ground bounce
- Reference planes: ground, power, return currents, splits
- High speed layout: vias, connectors, capacitors, losses
- Testing issues: equipment, probes, test points
- Models: SPICE, IBIS, drivers, receivers, simulators and accuracy
- PCB simulations that detect signal integrity problems before fabrication

*h) Education Requirements*

*AA or higher*

*i) Course Level*

*Entry Level, Engineering*

*j) Method of Instruction*

*On Campus, combinations of lecture and hand-on computer lab*

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## IC Packaging Fundamentals (EE-190)

*b) Objectives:*

This course provides an overview and a comparison of electronic systems packaging technologies. It includes design; manufacturing; test; IC package assembly; thermal and reliability issues. The course is developed around advanced design methodology and prepares the students for the entry-level position.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

Required: Fundamentals of Microsystems Packaging, by Rao Tummala, Publisher: McGraw-Hill Professional

*g) Course Outline*

**I Overview of IC Packaging Technology**
1. What is IC Packaging?
2. IC Packaging Roadmap
3. Technology Driving Forces
4. Rent's Rule
5. Hermatic vs. Nonhermatic Packages
6. Multidiscipline Issues

**II Manufacturing Considerations**
1. Die Attach Technology
2. Die Interconnect Technology
3. Die Coating
4. Plastic Package Manufacturing Process
5. Ceramic Package Manufacturing Process
6. Metal Can Package Manufacturing Process
7. Multichip Module
8. Environmental Control: ESD & Cleanroom Classification
9. Quality and Reliability Issues

**III Design Considerations**
1. Electrical
1.1 Reflection Noise
1.2 Crosstalk Noise
1.3 Switching Noise
1.4 Signal Attenuation and Dispersion
2. Thermal
2.1 Thermal Resistance
2.2 Heat Flow Mechanisms
3. Mechanical
3.1 Coefficient of Thermal Expansion (CTE)
3.2 Thermal Stress and Strain Distribution Management

**IV Electrical Test**
1. Electrical PerformanceTesting
2. Electrical Test Methods
3. Electrical Analysis

**V Emerging Technologies**
1. Ball Grid Array, Chip-scale package (CSP)
2. Flip Chip, Direct Chip Attach (DCA), Wafer Scale package (WSP)
3. 3D Packaging
4. Known Good Die

*h) Education Requirements*
*AA or higher*

*i) Course Level*
*Entry Level, Technician, Engineering*

*j) Method of Instruction*
*On Campus, combinations of lecture and hand-on computer lab*

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## IC Packaging Design Essentials (EE-192)

*b) Objectives:*

This course covers the design of packaging for integrated circuits. A description of the various IC packaging options is presented to allow the student to understand the trade-offs between different package types such as perimeter 10 packages versus area array packages. Wire bond and flipchip IC attachment methods are analyzed for physical characteristics such as wire bond pull strength and thermal expansion. Electrical effects of the IC package are analyzed through the use of lattice diagrams and impedance calculations and a description of the manufacturing of the three types of MCMs (MCM-D, MCM-L, and MCM-C) is explored.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

Required: Fundamentals of Microsystems Packaging, by Rao Tummala, Publisher: McGraw-Hill Professional

*g) Course Outline*

1. Introduction and Overview
1.1. Introduction to IC Packaging
1.2. Hierarchy of packaging
1.3. Importance of packaging and functions of the package
1.4. The multiple disciplines required for packaging
1.5. Introduction of package types
1.5.1. PGA
1.5.2. BGA
1.5.3. QFP
1.6. Introduction to advanced packaging technologies
1.6.1. Chip scale packaging
1.6.2. 3D high density packaging
1.6.3. PoP
1.6.4. System in package
1.7. Calculating packaging efficiency
1.8. Estimating 10 requirements using Rent's Rule
2. First Level Interconnect
2.1. Tradition packaging technologies
2.1.1. Wirebond
2.1.1.1.Wedge bonding
2.1.1.2.Ball stitch bonding
2.1.2. Flip Chip
2.1.2.1.Flip chip advantages over wirebond
2.1.2.2.Assembly of flip chip technology
2.1.2.3.Die bump functions
2.2. Wirebond pull strength
2.3. Expansion differentials. 3. Package Characteristics
3.1. Electrical characteristics
3.1.1. Define formulas for calculating impedance on a transmission line
3.1.1.1.Stripline
3.1.1.2.Microstrip
3.1.1.3.Buried stripline
3.1.2. Define formulas for calculating propagation delays.
3.1.3. Use lattice diagrams to analyze reflections.
3.2. Thermal Characteristics
3.2.1. Thermal transport modes
3.2.1.1.Conduction
3.2.1.2.Convection
3.2.1.3.Radiation
3.2.1.4.Newton's Law of Cooling 4. Packaging Design Flow
4.1. A Package Design flow
4.1.1. Modeling the package
4.1.2. Modeling the ICs
4.1.3. Wirebonding
4.1.4. Dynamic manufacturing constraints
4.1.5. Package interconnect and routing
4.1.6. Creating manufacturing data
5. Substrate Assembly
5.1. MCM types
5.1.1. Thin film (MCM-D)
5.1.2. Thick film (MCM-C)
5.1.3. Organic (MCM-L)
5.2. Manufacturing challenges
5.2.1. Etch factor
5.2.2. Planarization
5.3. Assembly techniques
6. Package Reliability and Failure Analysis
6.1. Overstress failures and wearout failures
6.2. Electrical failure mechanisms
6.3. Thermomechanical failure mechanisms
6.4. Chemically induced failure mechanisms
6.5. Multi-chip module yields

*h) Education Requirements*
*AA or higher*

*i) Course Level*
*Entry Level, Technician, Engineering*

*j) Method of Instruction*
*On Campus, combinations of lecture and hand-on computer lab*

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## Digital Signal Processing Principles and Applications (EE-200)

*b) Objectives:*

With signal processing becoming ubiquitous in today's computer literate world, a large number of application areas are growing in importance, both in industry and in the research community, such as signal processing for distributed sensor networks, speech, image and video processing, medical image processing, wavelets and multiresolution signal processing, genomic and biomedical signal processing, financial data signal processing, etc. This course will cover some of the theoretical, algorithmic and practical foundations needed to address this litany of problems and applications in signal processing.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

Digital Signal Processing: Principles, Algorithms, and Applications, Prentice-Hall
By J. G. Proakis and D. G. Manolakis
Ref: Statistical Digital Signal Processing and Modeling, Wiley, by Monson H. Hayes, (ISBN 0471594318)

*g) Course Outline*

- Signals, Systems, and Signal Processing
- Discrete-Time Signals and Systems
- The Z-transform and its Applications to the Analysis of LTI Systems
- Frequency Analysis of Signals and Systems
- The Discrete Fourier Transform: Its Properties and Applications
- Efficient Computation of the DFT: Fast Fourier Transforms (FFTs)
- Implementation of Discrete-Time Systems
- Design of Digital Filters: FIR/IIR

*h) Education Requirements*

BSEE or higher

*i) Course Level*

Entry Level, Engineering

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## Digital Signal Processing with MATLAB (EE-205)

*b) Objectives:*

This hands-on course explores the use of MATLAB for Design and Signal Processing. The course introduces various concepts of modern Digital Signal Processing, beginning with basic concepts in discrete time systems, filter design and implementation all the way to advanced concepts of multi-rate systems. In parallel, MATLAB is presented as a tool to verify the theory and SIMULINK to address design issues. Each session consists of a balanced mix of theory and practice.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

Digital Signal Processing Using Matlab, Edited by André Quinquis

*g) Course Outline*

- Introduction.
- Discrete-time signals.
- Discrete-time random signals.
- Statistical tests and high order moments.
- Discrete Fourier transform of discrete signals.
- Linear and invariant disctrete-time systems.
- Infinite impulse response filters.
- Finite impulse response filters.
- Detection and estimation.
- Power spectral density estimation.
- Time-frequency analysis.
- Parametrical time-frequency methods.
- Supervised statistical classification.
- Data compression.

*h) Education Requirements*

BSEE or higher

*i) Course Level*

Entry Level, Engineering

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## Embedded System Design Fundamentals (EE-207)

*b) Objectives:*

This course explores methodologies for systematic design of embedded systems including system specification, architecture modeling, component partitioning, estimation metrics, hardware software co-design. Embedded computing platforms and programming. The course further explains how to put all components of the system such as ASIC, CPU, and glue logic together.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

Embedded System Design: A Unified Hardware/Software Introduction, By Frank Vahid and Tony Givargis, John Wiley & Sons; ISBN: 0471386782

*g) Course Outline*

- Introduction. Design methodology and representation. Current CAD design. System-level design.
- Modeling. FSM models. Event Nets. Data Flow and Control Flow models. Flow Chart-based models. UML. Spec Charts. Uniprocessor and Multiprocessor systems. Application-Specific Architectures. Networks.
- ASIC. Specification and representation of embedded systems. HDL. Behavioral and Structural Hierarchy. Data-driven and Control-driven concurrency. Communication and synchronization. Timing. Logic synthesis algorithms.
- CPU. Embedded computing. ARM-based systems. Computing platform. Program design and analysis.
- Estimation and Verification. Estimation techniques at the system level. Simulation of system level design. Prototyping.
- Applications. Digital Camera, Wireless videophone, and others.

*h) Education Requirements*

MSEE, MSCS or higher

*i) Course Level*

Entry Level, Engineering

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## Practical Design with DSP (EE-209)

*b) Objectives:*

Advanced DSP (Digital Signal Processor) chips are increasingly being used to design sophisticated products for communications, instrumentations, etc. This hands-on course introduces the students to DSP system design and implementations using programmable signal processors. Several hand-on laboratory exercises, employing a widely used digital signal processor family, are used in conjunction with the lectures to present the design and implementation aspects.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, 6:00pm-9:00pm.

*f) Text Books*

Required: NA

*g) Course Outline*

- Signals and signal characteristics
- Discrete-time signals and systems
- Linear Systems: properties and characteristics, examples
- ADC and DAC: Sampling Theorem, Anti-alias Filter
- DSP Software: Fixed Point, Floating Point, Number Precision, Complex Numbers, Execution Speed
- Tools for DSP System Analysis and Design
- DSP Processors comparison
- TMS320F2812 DSP Architecture
- A DSP Development System TMDSEZD2812 F2812 eZdsp Starter Kit
- Code Composer Studio for DSP System Development
- Convolution: properties and applications
- Discrete Fourier Transform: spectral analysis of signals
- Fast Fourier Transform: some practical applications
- Fast Fourier Transform Implementation
- Frequency Domain Parameters, HP, LP, BP, and BR-Filters
- Finite Impulse Response (FIR) filter Implementation
- Infinite Impulse Response (IIR) filter Implementation
- Moving Average Filters
- Windowed-Sinc Filters
- Filter Comparison
- Audio Processing: Human Hearing, Hi-Fi Audio
- Hand-on Projects:
  - Architectural Overview of the DSK, Programming Development Environment familiarization
  - Peripheral Register Header Files, Reset and Interrupts, System Initialization
  - Analog-to-Digital Converter
  - FIR Filter
  - IIR Filter
  - FFT and spectrum analysis

*h) Education Requirements*

BSEE or higher

*i) Course Level*

Entry Level, Engineering

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## FPGA Design Fundamentals (EE-190)

*b) Objectives:*

This course is intended for designers new to FPGAs design or programmable logic. Beginning with the architecture of Xilinx and/or Altera FPGA, the course will first provide the essential knowledge required to implement a design successfully using the software tools. The first part of the course will give students a head start on not just a fast design turn, but an elegant design as well. The second part of the course focuses on how to create more efficient designs to enhance overall performance. Student will learn how to create a faster design, fit the design into a smaller FPGA or a lower speed grade, thereby reducing the system cost and development time.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

This course requires no text book.

*g) Course Outline*

- Basic FPGA Architecture
- Lab 1: Xilinx Tool Flow
- Reading Reports
- Lab 2: Architecture Wizard and PACE
- Global Timing Constraints
- Lab 3: Global Timing Constraints
- Implementation Options
- Lab 4: Implementation Options
- Synchronous Design Techniques Review of Fundamentals of FPGA Design
- Designing with Virtex-4 FPGA Resources
- CORE Generator Software System
- Lab 5: CORE Generator Software System
- Designing Clock Resources
- Lab 6: Designing Clock Resources
- FPGA Design Techniques
- Synthesis Techniques
- Lab 7: Synthesis Techniques Properties and Applications
- Achieving Timing Closure Timing Groups and OFFSET Constraints Lab 9: Achieving Timing Closure
- Advanced Implementation Options
- Lab 10: Designing for Performance
- Power Estimation (Optional)
- Lab 11: FPGA Editor Demo (Optional)
- ChipScope™ Pro Analyzer (Optional)
- Lab 12: ChipScope Pro Analyzer (Optional)

*h) Education Requirements*

BSEE or higher

*i) Course Level*

Entry Level, Engineering

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## Automated Test and Measurement with LabVIEW (EE-140)

*b) Objectives:*

This course is developed around using National Instrument's LabVIEW software and intends to teach students how to configure a wide variety of measurement, signal generation, RF, power, and switch modules in NI LabVIEW and other software to meet their specific test and measurement tasks.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

This course requires no text book.

*g) Course Outline*

- Identifying the steps in the software development
- method
- Defining a problem
- Designing an algorithm, flowchart, or state transition
- diagram
- Preparing for implementation, testing, and maintenance of applications
- Designing a user interface (LabVIEW front panel)
- Choosing data types and displaying data as a plot
- Using structures like the While loops and For loops
- Adding software timing to your code
- Making decisions in your code using case
- structures
- Documenting your code
- Plug-in DAQ devices – typical hardware
- characteristics
- Data acquisition in LabVIEW – software
- architectures
- Simulating a DAQ device
- Performing analog input and output
- Counters
- Performing digital input and output
- Single loop architectures – simple VI, general VI, and the state machine design patterns
- · Multiple loop architectures – parallel loop VI, the master/slave, and the producer/consumer design
- patterns
- · Parallelism
- · Adding timing to a design pattern
- VI server architecture
- · Property nodes
- · Control references
- · Invoke nodes

*h) Education Requirements*

BSEE or higher

*i) Course Level*

Entry Level, Engineering

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## Digital VLSI IC Design with Verilog (EE-210)

*b) Objectives:*

This hands-on course presents to the students the design of digital integrated circuits using the Verilog digital design language as described in IEEE Standard 1364-2001. By a balanced mixture of lectures and labs, the students are introduced to language constructs in a progressively more complex project environment. During the course, students will become familiar with the use of the Synopsys Design Compiler to synthesize gate-level netlists from behavioral, RTL, and structural Verilog code. The synthesis constraints most useful for area and speed optimization are emphasized. Almost all work is done in the synthesizable subset of the language; logic simulation is treated as an occasional verification method. Other topics include design partitioning, hierarchy decomposition, safe coding styles, assertion-based verification, and design for test.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

Required: M.D. Ciletti, "*Modeling, Synthesis, and Rapid Prototyping with Verilog HDL*" Prentice Hall,1999

Reference: D.E. Thomas and P. Moorby, "*The Verilog Hardware Description Language*" 3rd. Edition, KluwerAcademic Press, 1996.

*g) Course Outline*

- Modules and hierarchy
- Blocking/nonblocking assignment
- Combinational logic
- Sequential logic
- Behavioral modelling
- RTL modelling
- Gate-level modelling
- Hardware timing and delays
- Verilog parameters
- Basic system tasks
- Timing checks
- Generate statement
- Simulation event scheduling
- Race conditions
- Synthesizer operation
- Synthesizable constructs
- Netlist optimization
- Synthesis contol directives
- Verilog influence on optimization
- Use of SDF files
- Test structures
- Error correction basics
- Hand-on Projects:
    - shift and scan registers
    - counters
    - memory and FIFO models
    - digital phase-locked loop (PLL)
    - serial-parallel (and v-v) converter
    - serializer-deserializer (SerDes)
    - primitive gates
    - switch-level design
    - netlist backannotation

*h) Education Requirements*

BSEE or higher

*i) Course Level*

Entry Level, Engineering

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

**Timing Verification of Digital VLSI Designs (EE-215)**

*b) Objectives:*

This is a course covering timing verification during the complete netlist-to-tapeout backend flow in a typical suite of EDA tools. Simulation and other functional verification is held to a minimum.
A full-duplex serdes design totaling some 250,000 transistors equivalent, is used for the majority of exercises and illustrations requiring design hierarchy. Using the Synopsys® tools, synthesis constraints on the original verilog source first are explored in detail; then, the resulting netlist is floorplanned, placed-and-routed, and converted to a tape-out mask definition format. Static timing verification is exercised in all tools supporting it, at all stages of the process.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

Required: Bhatnagar, H. Advanced ASIC Chip Synthesis Using Synopsys. Design Compiler. Physical Compiler. and Primetime. Norwell, Massachusetts: Kluwer Academic, 2001.

*g) Course Outline*

- Basic tool flow from synthesis through tape-out. TcL and SDC in the Synopsys tools; TcL Basics; SDC Basics. The Milkyway database. HDL partitioning and optimization. Synthesizer scripts, design rules, and constraints. Clock constraints, delay constraints, and critical paths.
- HDL embedded synthesis scripts. Characterization of submodules. Advanced synthesis and optimization controls. Technology-library modelling. Basics of Liberty syntax and Liberty-ALF similarities. Cell characterization overview. Design netlist and extracted models. QTM models.
- Design interface-logic models (ILM) vs extracted HTV models. Design-block STAMP models. STAMP syntax and extracted STAMP models.
- The JupiterXT floorplanner, design flow, and the Flow Manager. Flat vs hierarchical floorplans, placement plan groups, and pad placement. Cells, flylines, and floorplan reports. Jupiter feasibility analysis, back-annotation, and constraints. SDF coordination.
- Incremental resynthesis. Jupiter ECO's. Astro Introduction. Floor-planning and incremental changes. PrimeTime with a floor-plan; PrimeTime ECO's.
- Fully-placed timing verification. Placement legalization, global routing, and final-placement flow. Clock tree timing and use of the IC Compiler.
- IC Compiler and fully-placed SDF. SPEF features and basic parameters.
- PrimeTime and placement. Detailed routing flow.
- IC Compiler features and constraints. Parasitics, crosstalk, and timing. Pin separation and extraction of HTV timing.
- Effects of routing on timing. PrimeTime fully-routed verification. PrimeTime ECO of final netlist.
- Tape-out conversion; mask-definition formats; automated GDS2 or OASIS generation.

*h) Education Requirements*

BSEE or higher

*i) Course Level*

Entry Level, Engineering

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

**Design of Digital CMOS Integrated Circuits (EE-300)**

*b) Objectives:*

This course provides a detailed review of the principles, concepts, and design methods used in the design of basic digital circuits using CMOS technology. The course will begin with a brief review of background information (i.e. fabrication technology, CMOS device physics, and related device equations), and then proceed to common digital building blocks and more complex digital circuits. Computer simulations are be used extensively to enhance the learning experience.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

CMOS DIGITAL INTEGRATED CIRCUITS by Kang and Leblebici, ISBN: 0072460539, San Francisco, McGraw-Hill

*g) Course Outline*

- Basics of MOSFET operation and SPICE modeling
- MOS inverters: static characteristics
- MOS inverters: dynamic operation
- CMOS Layout and Simulation
- Combinational MOS logic circuits
- Sequential MOS logic circuits
- Dynamic MOS logic circuits
- Semiconductor memories

*h) Education Requirements*

BSEE or higher

*i) Course Level*

Entry Level, Engineering

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

**Design of Analog CMOS Integrated Circuits (EE-310)**

*b) Objectives:*

Modern integrated circuit design is broadly divided into analog and digital design. This course provides a detailed review of the principles, concepts, and design methods used in the design of current state-of-the-art CMOS analog circuits. The course will begin with a brief review of background information (i.e. fabrication technology, CMOS device physics, and related device equations), and then proceed to common analog building blocks and more complex analog circuits. Computer simulations are be used extensively to enhance the learning experience.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

CMOS Analog Circuit Design
by Phillip E. Allen and Douglas R. Holberg
ISBN: 0-19-510720-9

*g) Course Outline*

- Introduction/Review of symbols, terminology, and circuit notation of analog systems.
- Overview of process technology, and fabrication steps. The PN junction, device physics/carrier concentrations and related equations. The MOS transistor and it's 4-terminal operation/related equations. Properties of MOS capacitors, and resistors.
- Large-Signal FET model. Output characteristics of MOS transistor. Nonideal/parasitic device models/effects within MOS transistor. Small-Signal FET model.
- Analog building blocks: MOS switch, active resistors/loads, voltage dividers, current sinks/sources, cascode current sink, current mirrors, cascode current mirrors, Wilson current mirrors, current/voltage references, and bootstrap references.
- Amplifiers: simple inverters, current-sink inverter, push-pull inverters, differential amplifiers, cascode amplifiers, simple output amplifiers, source-follower amplifiers, push-pull source follower, and high gain amplifiers.
- Comparators: first order models, inverting comparators, differential input comparators, two-stage comparators, comparator hysteresis, and auto-zeroing techniques.
- Operational Amplifiers: non-ideal models, frequency response, compensation, two-stage operational amplifiers, cascode operational amplifiers, differential Cascade stages, cascode output stages, calculation of power supply rejection ratios, folded cascode operational amplifiers, open loop characteristics, common mode rejection ratios, and common mode gain

*h) Education Requirements*

BSEE or higher

*i) Course Level*

Entry Level, Engineering

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*
**Advanced Analog CMOS IC Design (EE-310)**

*b) Objectives:*
Modern integrated circuit design is broadly divided into analog and digital design. This course provides a detailed review of the principles, concepts, and design methods used in the design of current state-of-the-art CMOS analog circuits. The course will begin with a brief review of background information (i.e. fabrication technology, CMOS device physics, and related device equations), and then proceed to common analog building blocks and more complex analog circuits. SPICE simulations will be used extensively to augment the text/lecture material.

*d) Length of program:*
The course duration is 12 weeks.

*e) Class Sessions*
Classes are being held twice a week, typically 3 hours each.

*f) Text Books*
CMOS Analog Circuit Design
by Phillip E. Allen and Douglas R. Holberg
ISBN: 0-19-510720-9

*g) Course Outline*

- Introduction/Review of symbols, terminology, and circuit notation of analog systems.
- Overview of process technology, and fabrication steps. The PN junction, device physics/carrier concentrations and related equations. The MOS transistor and it's 4-terminal operation/related equations. Properties of MOS capacitors, and resistors.
- Large-Signal FET model. Output characteristics of MOS transistor. Nonideal/parasitic device models/effects within MOS transistor. Small-Signal FET model.
- Analog building blocks: MOS switch, active resistors/loads, voltage dividers, current sinks/sources, cascode current sink, current mirrors, cascode current mirrors, Wilson current mirrors, current/voltage references, and bootstrap references.
- Amplifiers: simple inverters, current-sink inverter, push-pull inverters, differential amplifiers, cascode amplifiers, simple output amplifiers, source-follower amplifiers, push-pull source follower, and high gain amplifiers.
- Comparators: first order models, inverting comparators, differential input comparators, two-stage comparators, comparator hysteresis, and auto-zeroing techniques.
- Operational Amplifiers: non-ideal models, frequency response, compensation, two-stage operational amplifiers, cascode operational amplifiers, differential Cascade stages, cascode output stages, calculation of power supply rejection ratios, folded cascode operational amplifiers, open loop characteristics, common mode rejection ratios, and common mode gain

*h) Education Requirements*
BSEE or higher

*i) Course Level*
Entry Level, Engineering

*j) Method of Instruction*
On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*
Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## Design of Radio Frequency Integrated (RFIC) Circuits (EE-330)

*b) Objectives:*

This program covers the design techniques, devices, tools and methodologies for design of integrated radio frequency circuits. The course introduces the students to the current wireless transceiver architectures and provides the students with deep insight into the physics, characteristics and design of passive components (inductor, capacitor) and active devices. This course will further trains the students in the IC design for advanced RF applications such as high speed amplifiers, LNA, Mixer, VCO, PA, PLL and synthesizers.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

Required: Thomas H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 1998.
Reference: Behzad Razavi, *RF Microelectronics*, Prentice-Hall 1998

*g) Course Outline*

- Introduction to Radio Frequency Integrated Circuits and wireless transceiver architectures
- Physical quantities and their logarithmic representations: dB, dBm, dBV, dBA
- Devices: diode, BJT, MOS
- Modeling of passive/active integrated devices
- Signal sources: ideal vs. real.
- Limitations of analog circuits:
    - Noise & distortion.
    - Nonlinear distortion
- Measures of distortion:
    - Compression
    - Desensitization
    - Inter-modulation
- Nonlinearity and negative feedback.
- Overview of monolithic bipolar and CMOS:
    - LNA's
    - Mixers
    - Filters
    - Broadband amplifiers
    - RF power amplifiers
    - VCO's, and frequency synthesizers
- Analysis of noise and non-linearity in RFIC's

*h) Education Requirements*

BSEE or higher

*i) Course Level*

Entry Level, Engineering

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## Advanced RFIC Design (EE-340)

*b) Objectives:*

This program covers the design techniques, devices, tools and methodologies for design of integrated radio frequency circuits. The course introduces the students to the current wireless transceiver architectures and provides the students with deep insight into the physics, characteristics and design of passive components (inductor, capacitor) and active devices. This course will further trains the students in the IC design for advanced RF applications such as high speed amplifiers, LNA, Mixer, VCO, PA, PLL and synthesizers.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

Required: Thomas H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits,* Cambridge University Press, 1998.
Reference: Behzad Razavi, *RF Microelectronics*, Prentice-Hall 1998

*g) Course Outline*

- Introduction to Radio Frequency Integrated Circuits and wireless transceiver architectures
- Physical quantities and their logarithmic representations: dB, dBm, dBV, dBA
- Devices: diode, BJT, MOS
- Modeling of passive/active integrated devices
- Signal sources: ideal vs. real.
- Limitations of analog circuits:
- Noise & distortion.
- Nonlinear distortion
- Measures of distortion:
- Compression
- Desensitization
- Inter-modulation
- Nonlinearity and negative feedback.
- Overview of monolithic bipolar and CMOS:
- LNA's
- Mixers
- Filters
- Broadband amplifiers
- RF power amplifiers
- VCO's, and frequency synthesizers
- Analysis of noise and non-linearity in RFIC's

*h) Education Requirements*

BSEE or higher

*i) Course Level*

Entry Level, Engineering

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## Design of Low Power Digital Integrated Circuits (EE-350)

*b) Objectives:*

This course introduces students to IC design for low power and energy consumption. Some of the topics covered are: Low power architectures, logic styles, and circuit design. Variable supply and threshold voltages. Leakage management. Power estimation. Energy sources, power electronics, and energy recovery. Course will also include applications in portable electronics and sensors, and Thermodynamic limits.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

Required: Low Power Design Essentials (Integrated Circuits and Systems) by Jan Rabaey
Reference: Roy, K. and Prasad, S., Low Power CMOS VLSI: Circuit Design
Chandrakasan, A. and Broderson, R., eds., Low-Power CMOS Design

*g) Course Outline*

- Overview of Low Power Design
  - CMOS Power Dissipation
  - Power and Performance Tradeoffs
  - Trends in IC Power Consumption
- Low Power Architectures
  - Clock Gating and Clock Management
  - Pipelining to Reduce Supply Voltage
  - Parallelization to Reduce Supply Voltage
- Low Power Circuit Design
  - Logic Power Estimation
  - Power Minimization in Static CMOS
  - Power Minimization in Dynamic CMOS
  - Multiple-Threshold CMOS
  - Variable Supply and Threshold Voltages
  - Managing Leakage
  - Subthreshold Circuit Design
  - Silicon-on-Insulator (SOI) Technologies
  - Energy Recovery
  - Interconnect Power Estimation and Management
- Energy Sources and Power Electronics
  - Batteries and Fuel Cells
  - Energy Scavenging
  - DC/DC Converters: Fundamentals
  - DC/DC Converters: Optimization
- Other Topics in Low Power Design
  - Low Power Synthesis
  - Applications: Computing, Communication, and Multimedia
  - Applications: Sensors and Sensor Networks
  - Fundamental Limits and Thermodynamics of Computation

*h) Education Requirements*

BSEE or higher

*i) Course Level*

Entry Level, Engineering

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

*a) Course Title:*

## Low Power VLSI Design (EE-370)

*b) Objectives:*

The course explores in adequate detail various practical design methodologies for improving the power performance of SoC products. Among the design concepts covered in this course are: Clock Gating, Power Gating, Multivoltage Designs, Multi-threshould techniques, etc. In addition to lecture notes in PowerPoint, course includes several detailed labs where students can gain a closer understanding of the concepts and become familiar with the underlying design methodologies and flows.

*d) Length of program:*

The course duration is 12 weeks.

*e) Class Sessions*

Classes are being held twice a week, typically 3 hours each.

*f) Text Books*

Required: Low power VLSI design manual co-authored by ARM, Renesas and Synopsys

*g) Course Outline*

- Power vs. Energy
- Dynamic Power
- Conflict between Dynamic and Static Power
- Static Power
- Clock Gating
- Gate Level Power Optimization
- Multi VDD
- Multi-Threshold Logic
- Challenges in Multi-Voltage Designs
- Voltage Scaling Interfaces – Level Shifters
- Automation and Level Shifters
- Level Shifter Recommendations and Pitfalls
- Timing Issues in Multi-Voltage Designs
- Power Planning for Multi-Voltage Design
- System Design Issues with Multi-Voltage Designs
- Level Shifters – High to Low Voltage Translation
- Level Shifters – Low-to-High Voltage
- Level Shifter Placement
- Dynamic and Leakage power profiles
- Principles of Power Gating Design
- Power Switching – Fine Grain vs. Coarse Grain
- The Challenges of Power Gating
- Impact of Power Gating on Classes of Sub-systems
- Switching Fabric Design
- Signal Isolation
- State Retention and Restoration Methods
- Power Gating Control
- Power Gating Design Verification
- Design For Test considerations
- Hierarchy and Power Gating
- Power State Tables and Always On Regions
- Power Networks and Their Control
- On-chip Power Gating
- External Power Rail Switching
- Fundamental Limits

*h) Education Requirements*

BSEE or higher

*i) Course Level*

Entry Level, Engineering

*j) Method of Instruction*

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

APPENDIX –II

This appendix contains the listing and qualification of additional CalPT faculty

## Additional CalPT Faculty

**Faculty Name: Dr. Ali Iranmanesh**

1. **Educational Background:**
    a. **Earned Degree: Ph.D., Electronics and Physics**
    b. **Name of the Institution awarding the above Degree: Stanford University**
    c. **Date degree was granted: June 1984**
2. **Fields of specialization: Semiconductor Technology, Device Physics, IC Circuits Design**
3. **Teaching, research and, administrative experience: Over 10 years teaching experience in Silicon Valley Technical Institute. Over 25 years experience in high-tech industry in area of IC circuit design and semiconductor technology.**
4. **Teaching assignments for the current year:**
    a. **Advanced Analog CMOS IC Design (EE-320)**
    b. **Design of Radio Frequency Integrated Circuits (EE-330)**
    c. **Advanced RFIC Design (EE-340)**
    d. **Design of Low Power Digital Integrated Circuits (EE-350)**
    e. **Low Power VLSI Design (EE-370)**
5. **Other duties assigned for the current year.**
    a. **School Director**
6. **The institution shall describe the faculty's role in curriculum development**
    a. **Responsible for curriculum development**

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**Faculty Name: Dr. John Michael Williams**

1. **Educational Background:**
    a. **Earned Degree: Ph.D. Philosophy**
    b. **Name of the Institution awarding the above Degree: Carbondale, Illinois, 62901**
    c. **Date degree was granted: June 1980**
2. **Fields of specialization: Information Technology, Verilog, C, C++, Digital Design**

3. **Teaching, research and, administrative experience: Over 5 years teaching experience in Silicon Valley Technical Institute. Over 25 years experience in high-tech industry in area of high-Level design methodologies.**

4. **Teaching assignments for the current year:**

    a. **Software Quality Assurance Essentials (CS-150)**
    b. **FPGA Design Fundamentals (EE-190)**
    c. **Digital VLSI IC Design with Verilog (EE-210)**
    d. **Timing Verification of Digital VLSI Designs (EE-215)**

5. **Other duties assigned for the current year.**
    a. **None**

6. **The institution shall describe the faculty's role in curriculum development**
    a. **None**

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**Faculty Name: Dr. Kris Verma**

1. **Educational Background:**

    a. **Earned Degree: Ph.D. in EE**

    b. **Name of the Institution awarding the above Degree: University of Utah, Salt Lake City, Utah**

    c. **Date degree was granted: 1972**

2. **Fields of specialization: Semiconductor Devices , Process Technology ,& wafer Manufacturing in Mega foundries, Microwave/Wireless, IC design layout and Design services**

3. **Teaching, research and, administrative experience: Over 6 years teaching at Silicon Valley Technical Institute. Life time Teaching Certificate from State of California, issued in 1972. Over 30 years in Electronics High Tech Industries ( Silicon Valley, CA)**

4. **Teaching assignments for the current year:**

    a. **Solar Photovoltaic System Design Essentials (EN-100)**
    b. **Advanced Solar Photovoltaic System Design (EN-120)**
    c. **Advanced Semiconductor Devices - Physics & TCAD (SS-200)**
    d. **Solar Photovoltaic Device Physics (SS-210)**

e. **Advanced Semiconductor Technology and Fabrication (SS-220)**

5. **Other duties assigned for the current year.**
   **None**

6. **The institution shall describe the faculty's role in curriculum development**
   **None**

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**Faculty Name: Dr. Duvan Luong**

1. **Educational Background:**

   a. **Earned Degree: Ph.D., Computer and Information Science**

   b. **Name of the Institution awarding the above Degree: Lehigh University, Bethlehem, PA**

   c. **Date degree was granted: June 1987**

2. **Fields of specialization: Over 20 years in software development process, Quality Assurance**

3. **Teaching, research and, administrative experience: Over 5 years teaching experience in Silicon Valley Technical Institute. Over 25 years experience in high-tech industry in area of high-Level design methodologies.**

4. **Teaching assignments for the current year:**

   a. **Computer and Network Security Essentials (CIE-150)**
   b. **Software Quality Assurance Essentials (CS-150)**
   c. **Applied Electricity and Electronics Fundamentals (EE-100)**

5. **Other duties assigned for the current year.**
   a. **None**

6. **The institution shall describe the faculty's role in curriculum development**
   a. **None**

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**Faculty Name: Dr. Phillip H. Fischer**

7. **Educational Background:**

   a. **Earned Degree: Ph.D., Solid State Physics**

b. **Name of the Institution awarding the above Degree: Dartmouth College**

c. **Date degree was granted: June 1990**

8. **Fields of specialization: IC Circuits Design**

9. **Teaching, research and, administrative experience: Over 4 years teaching experience in Silicon Valley Technical Institute. Over 20 years experience in high-tech industry in area of IC circuit design.**

10. **Teaching assignments for the current year:**

    a. **IC Layout Design (EE-150)**
    b. **IC Layout Verification (EE-160)**
    c. **MEMS Design & Technology Fundamentals (EE-170)**
    d. **Design of Digital CMOS Integrated Circuits (EE-300)**
    e. **Design of Analog CMOS Integrated Circuits (EE-310)**

11. **Other duties assigned for the current year.**
    a. **None**

12. **The institution shall describe the faculty's role in curriculum development**
    a. **None**

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**Faculty Name: Dr. William Kao**

1. **Educational Background:**

    a. **Earned Degree: Ph.D. in EE**

    b. **Name of the Institution awarding the above Degree: U. of Illinois, Urbana-Champaign**

    c. **Date degree was granted: June 1979**

2. **Fields of specialization: Electronic design automation, green energy, solar energy**

3. **Teaching, research and, administrative experience: Over 10 years teaching experience in UCLA and Silicon Valley Technical Institute. Over 25 years experience in high-tech industry in area of electronic design automation, and green energy.**

4. **Teaching assignments for the current year:**

    a. **Software Quality Assurance Essentials (CS-150)**

b. **Solar Photovoltaic System Design Essentials (EN-200)**
c. **Advanced Solar Photovoltaic System Design (EN-120)**
d. **Solar Photovoltaic Device Physics (SS-210)**
e. **National Electrical Code (NEC) Training (EE-110)**

5. **Other duties assigned for the current year.**
    a. **None**

13. **The institution shall describe the faculty's role in curriculum development**
    a. **None**